
EM78M612

**Universal Serial Bus
Microcontroller**

**Product
Specification**

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.


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Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial Version	2003/03/05
1.1	<ol style="list-style-type: none"> 1. Made modifications on the General Description, and changed the ROM size from 12K→2K 2. Made modifications on the Pin Configuration of EM78M612XBP 3. Modified the ADC Converter Channel Selector Table 4. Added PDA Register Description 5. Made modifications on the EEPROM Function Description 6. Made modification on the PDA Function Description 7. Revised ADC Converter ready bit for ADC Operation 	2004/04/28
1.2	<ol style="list-style-type: none"> 1. Made modification on the Features, and changed the ROM size from 2048K×13→2048×13 bit 2. Made modification on the PWM description 3. Made modification on the ADC description 4. Made modifications on the Special Purpose Registers 5. Made modifications on the RAM Bank description 6. Modified the RES default value 7. Modified the CONT register description 8. Modified the IOC6 description 9. Modified the IOC9 description 10. Modified the IOCB, IOCC description 11. Modified the IOC8S description 12. Modified the DC Electrical Characteristic 13. Added Application Circuit 14. Added Appendix A ~ D 	2006/03/21
1.3	<ol style="list-style-type: none"> 1. Modified the package type 2. Modified the VDD operating voltage range 	2007/10/01
1.4	<ol style="list-style-type: none"> 1. Modified the package type 2. Added Appendix E ~ F 3. Added PDA, PWM, EEPROM application web link 	2008/10/09





1 General Description

The EM78M612 is a series of 8-bit Universal Serial Bus RISC architecture, Multi-Time Programming (MTP) microcontroller. It is specifically designed for USB low speed device application and supports legacy devices such as PS/2 mouse. The EM78M612 also supports one device address and two endpoints. With no firmware involved, these series of microcontrollers can automatically identify and decode Standard USB Command to Endpoint Zero.

The EM78M612 has five-level stacks and eight interrupt sources. It has a maximum of 15 General Input/Output pins. Each device has 112 bytes SRAM and is embedded with 4 bytes of E²PROM. The ROM size of the EM78M612 is 2K.

These series of ICs have special features that meet user's requirements. Such features are:

- Dual Clock mode which allows the device to run on very low power saving frequency.
- Pattern Detecting Application function which is used in a serial transmission to count waveform width.
- Width Modulation that can generate a duty-cycle-programmable signal.
- AD converter with up to 10 bits resolution.

2 Features

- Low-cost solution for low-speed USB devices, such as mouse, joystick, and game pad.
- USB Specification Compliance
 - Universal Serial Bus Specification Version 1.1
 - USB Device Class Definition for Human Interface Device (HID), Firmware Specification Version 1.1
 - Supports 1 device address and 2 endpoints
- USB Application
 - USB protocol handling
 - USB device state handling
 - Identifies and decodes Standard USB commands to EndPoint Zero



- PS/2 Application Support
 - Auto-detects PS/2 or USB port
 - Built-in PS/2 port interface
- Built-in 8-bit RISC MCU
 - 5-level stacks for subroutine nesting and interrupt
 - 8 available interrupts
 - 8-bit real time clock/counter (TCC) with overflow interrupt
 - Built-in RC oscillator free running for Watchdog Timer and Dual clock mode
 - Two independent programmable prescalers for WDT and TCC
 - Two methods of power saving:
 - Power-down mode (Sleep mode)
 - Low frequency mode
 - Two clocks per instruction cycle
 - Multi-time programmable
- I/O Ports
 - Up to 15 general-purpose I/O pins grouped into two ports (Port 6 and 7).
 - Up to 2 LED sink pins
 - Each GPIO pin of Ports 6 has an internal programmable pull-high resistor (200 K Ω)
 - Each GPIO pin wakes up the MCU from sleep mode by input state change
- Internal Memory
 - Built-in 2048 \times 13 bits Program ROM
 - Built-in 112 bytes general purpose registers (SRAM)
 - Built-in USB Application FIFOs
 - Built-in 4 bytes E²PROM (EM78M612*B, EM78M612*D)
- Operation Frequency
 - Normal Mode: MCU runs on the external oscillator frequency
 - Dual Clock Mode: MCU runs at the frequency of 256kHz (or 32kHz, 4kHz, 500Hz), emitted by the internal oscillator with the external ceramic resonator (or crystal) turned off to conserve power.
- Built-in Pattern Detecting Application for serial signal transmission
- Built-in Pulse Width Modulation (PWM)
 - Up to 2 channels PWM function on P.64 (PWM1) and P.65 (PWM2)
 - Up to 8-bit resolution of PWM duty cycles
 - Up to 8 selections of PWM frequency



- Built-in 15-Channel Analog-to-Digital Converter (ADC)
 - Built-in AD Converter with 10-bit resolution
 - 4 ADC conversion rates: 20K/10K/5K/2.5K
- Built-in 3.3V Voltage Regulator
 - For MCU power supply
 - Pull-up source for the external USB resistor on D-pin
- Package Type
 - 16-pin PDIP 300mil EM78M612 (A/D) AP
 - 16-pin SOP 150mil EM78M612 (A/D) AM
 - 18-pin PDIP 300mil EM78M612 (A/D) BP
 - 18-pin SOP 300mil EM78M612 (A/D) BM
 - 20-pin PDIP 300mil EM78M612 (A/D) CP
 - 20-pin SOP 300mil EM78M612 (A/D) CM
 - 20-pin SSOP 150mil EM78M612 (A/D) GM
 - 24-pin PDIP 600mil EM78M612 (A/D) DP
 - 24-pin PDIP 300mil EM78M612 (A/D) DK
 - 24-pin SOP 300mil EM78M612 (A/D) DM
 - 24-pin SSOP 150mil EM78M612 (A/D) HM
 - 32-pin QFN 5*5*0.8mm EM78M612 (A/D) AW

3 Pin Assignment

3.1 Function Type Description

The EM78M612 series has several types of packaging. Each type is divided into two modules, namely; without E²PROM and A/D Converter and with E²PROM and A/D Converter. Hence, packaging configuration for each series is defined. Table 3.1 below summarizes which series of the EM78M612 belong to which module.

Table 3-1 Packaging Summary of EM78M612 Series IC

Without E ² PROM and A/D Converter	With E ² PROM and A/D Converter
EM78M612A * *	EM78M612D * *

3.2 Pin Configuration

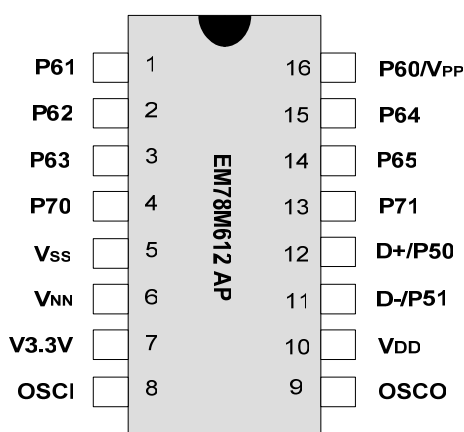


Figure 3-1 EM78M612AP

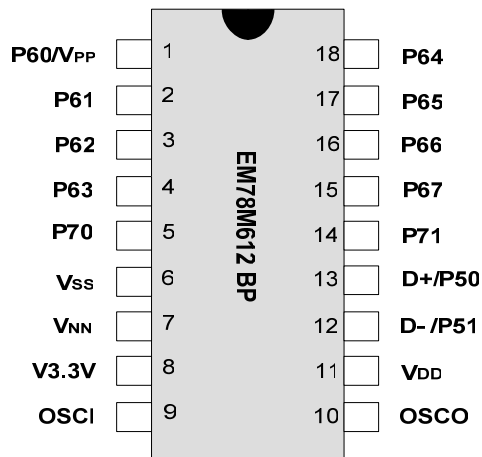


Figure 3-2 EM78M612BP

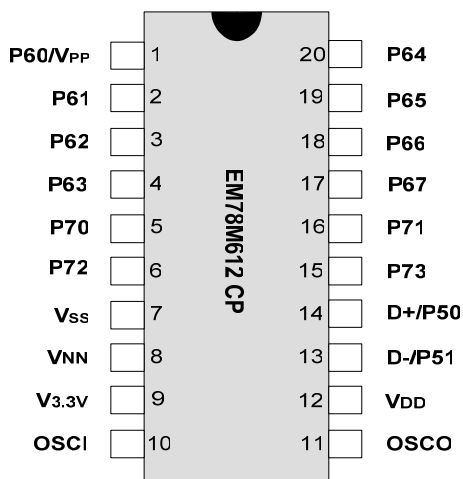


Figure 3-3 EM78M612CP

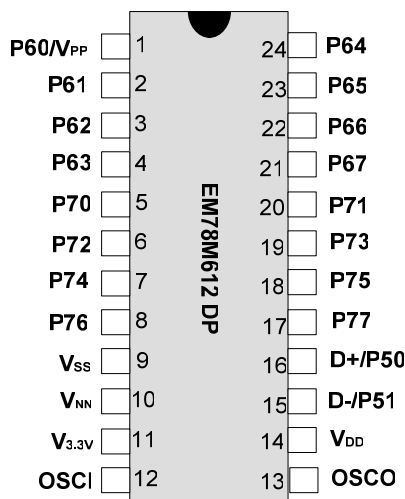


Figure 3-4 EM78M612DP

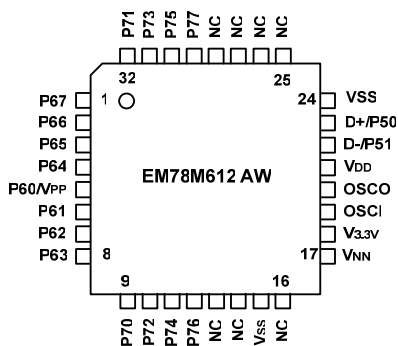


Figure 3-5 EM78M612 *AW

3.3 Pin Description

Symbol	I/O	Function
P60/VPP	I	P60 functions as an input pin only (no output) For serial signal transmission application, Pin P60 is used as a serial signal input pin. For detailed usage and function, refer to Section 8.8, Pattern Detecting Application of this Spec.
P61 ~ P67	I/O	7 GIOP pins. The pull high resistors (200K Ω) and pull low resistors (15K Ω) are selected through pin programming. P61 ~ P67 are used for AD function. Furthermore, P64 and P65 can also be used for PWM function, 3.3V I/O level.
P70 ~ P77	I/O	Port 7 offers up to 8 GIOP pins. The sink current of P70 and P71 are programmable for driving an LED. Each pin has pull high resistors (200K Ω) that can be selected through pin programming. All Port 7 I/O pins can be used for AD function. 3.3V I/O level.
D+ / P50	I/O	USB Plus data line interface or PS/2 line interface are user-defined through firmware setting. When this pin is used as a PS/2 line interface, it will generate an interrupt when its state changes.
D- / P51	I/O	USB Minus data line interface or PS/2 line interface are user-defined through firmware setting. When this pin is used as a PS/2 line interface, it will generate an interrupt when its state changes.
OSCI	I	6MHz / 12MHz ceramic resonator or crystal input.
OSCO	I/O	Return path for 6-MHz / 12MHz ceramic resonator or crystal.
VNN	-	Used in programming the on-chip ROM. During normal operation, this pin is connected to Ground.
V3.3V	O	3.3V DC voltage output from internal regulator. This pin has to be tied to a 4.7 μ F capacitor.
VDD	-	Connect to the USB power source or to a nominal 5V-power supply. Actual VDD range can vary between 4.4V and 5.5V.
VSS	-	Connect to ground.

4 Block Diagram

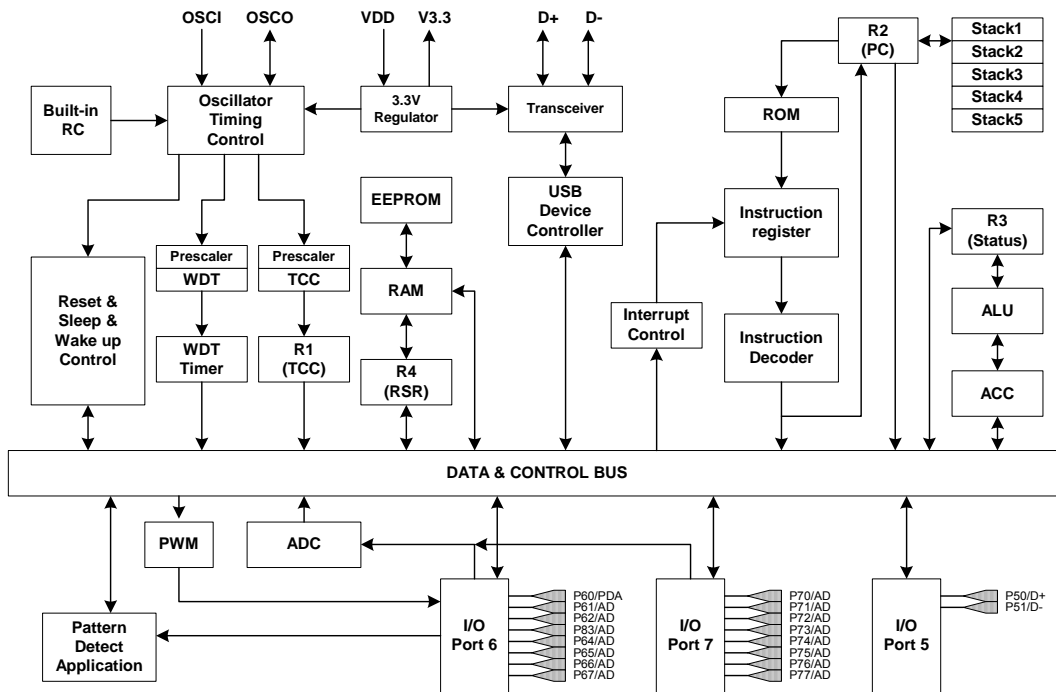


Figure 4 EM78M612 Series Function Block Diagram

5 Functional Description

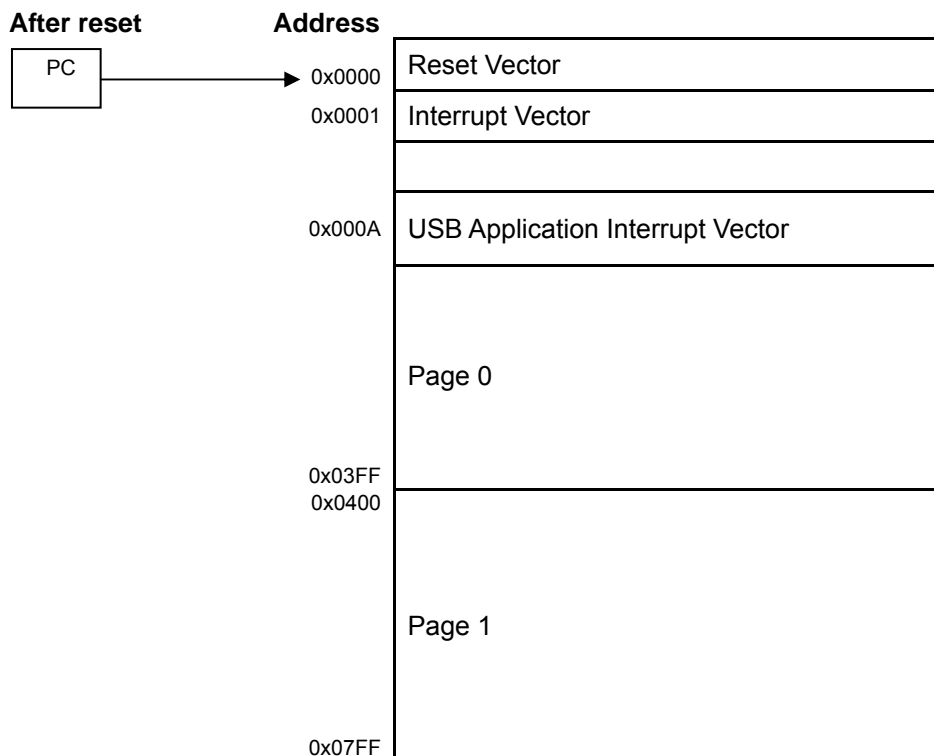
The EM78M612 memory is organized into four spaces, namely; User Program Memory in 2048×13 bits ROM space, Data Memory in 112 bytes SRAM space, and USB Application FIFOs (for Endpoint 0 and Endpoint 1). Furthermore, several registers are used for special purposes.

5.1 Program Memory

The program space of the EM78M612 is 2K bytes which is divided into two pages. Each page is 1K bytes long. After a Reset, the 11-bit Program Counter (PC) points to location zero of the program space.

It has two interrupt vectors, i.e., Interrupt Vectors at 0x0001 and USB Application Interrupt Vectors at 0x000A. The Interrupt Vector (0x0001) applies to TCC Interrupt, High Pattern Detecting Interrupt, Low Pattern Detecting Interrupt, and Port 5 State Changed Interrupt. The USB Application Interrupt Vector is for USB Endpoint Zero Interrupt, USB Suspend Interrupt, USB Reset interrupt, and USB Host Resume Interrupt.

After an interrupt, the MCU will fetch the next instruction from the corresponding address as illustrated in the following diagram.



5.2 Data Memory

The Data Memory has 112 bytes SRAM space. It is also equipped with USB Application FIFO space for USB Application. Figure 5-1 shows the organization of the Data Memory Space.

5.2.1 Special Purpose Registers

When the microcontroller executes instruction, specific registers are involved in the operation, such as; Status Register which records the calculation status, Port I/O Control Registers which control the I/O pins' direction, etc.

There are 22 Special Operation Registers which are located from Address 0x00 to 0x0F in Bank 0, and from Address 0x08 to 0x0E in Bank 1. Seventeen Special Control Registers are available to control functions I/O direction. These are arranged from Address 0x05 to 0x0F in Bank 0, and from Address 0x08 to 0x0F in Bank 1.

Note that Special Control Registers can only be read or written to by two instructions; IOR and IOW. To access registers from Bank 1, the Special Purpose Registers Bank selector (R3 [7]) should be set first.

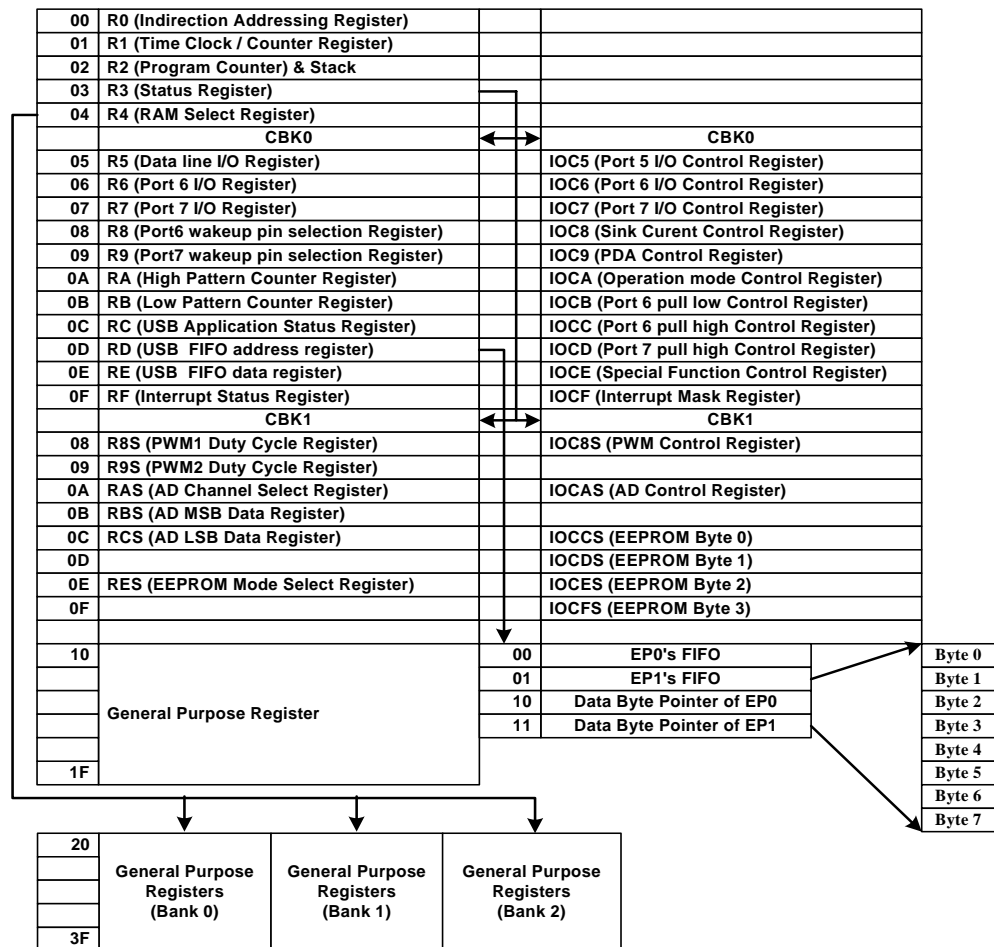


Figure 5-1 EM78M612 Data RAM Organization

5.2.1.1 Operation Registers in Bank 0

The following are the Operation Registers under the Special Purpose Registers in Bank 0. These Operation Registers are arranged according to the order of the registers' address. Note that some registers are read only, while others are both readable and writable.

R0 (Indirect Address Register) Default Value: (0B_0000_0000)

R0 is not a physically implemented register. It functions as an indirect address pointer. Any instruction using R0 as a pointer actually accesses the data pointed by the RAM Select Register (R4).

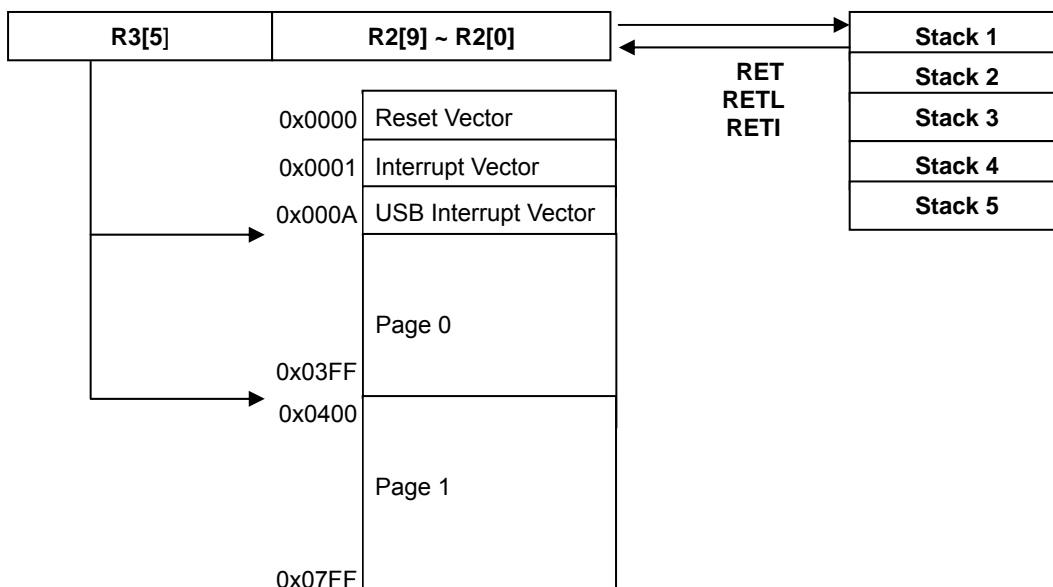
R1 (Time / Clock Counter) Default Value: (0B_0000_0000)

The TCC register is an 8-bit timer or counter. It is readable and writable as any other register.

After Power-on reset and Watchdog reset, the initial value of this register is 0x00.

R2 (Program Counter & Stack) Default Value: (0B_0000_0000)

The EM78M612 Program Counter is an 11-bit long register that allows access to 2K bytes of Program Memory. The Program Counter is cleared after Power-on reset or Watchdog reset. The first instruction that is executed after a reset is located at Address 00h.



R3 (Status Register) Default Value: (0B_0001_1000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPRBS	-	PS0	T	P	Z	DC	C

R3 [0] Carry flag

R3 [1] Auxiliary carry flag

R3 [2] Zero flag. It will be set to 1 when the result of an arithmetic or logic operation is zero.

R3 [3] Power down flag. It will be set to 1 during Power-on phase or by “WDTC” command and cleared when the MCU enters into Power-down mode. It remains in its previous state after a Watchdog Reset.

“0” : Power-down mode

“1” : Power on

R3 [4] Time-out flag. It will be set to 1 during Power-on phase or by “WDTC” command. It is reset to 0 by WDT time-out.

“0” : Watchdog timer with overflow

“1” : Watchdog timer without overflow

The various states of Power down flag and Time-out flag at different conditions are shown below:

T	P	Condition
1	1	Power-on reset
1	1	WDTC instruction
0	*P	WDT time-out
1	0	Power down mode
1	0	Wakeup caused by port change during Power down mode

* P: Previous status before WDT reset

R3 [5] Page selection bit. This bit is used to select a page of program memory (refer to R2, Program Counter).

PS0	Program Memory Page [Address]
0	Page 0 [0000-03FF]
1	Page 1 [0400-07FF]

R3 [6] General purpose registers.

R3 [7] Special purpose registers bank selector.

“0” : R5 ~ RF; IOC5 ~ IOCF

“1” : R8S ~ RFS; IOC8S ~ IOCFS

R4 (RAM Select Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BK1	BK0	Ad5	Ad4	Ad3	Ad2	Ad1	Ad0

R4 (RAM select register) contains the address of the registers.

R4 [0~5] are used to select registers in 0x00h~0x3Fh. The address 0x00~0x1F is a common space. After 0x1Fh, SRAM is grouped into three banks.

R4 [6, 7] are used to select register banks. To select a register bank, refer to the following examples and the table below:

R4=00001100 points and R4=01001100 point to the same register 0x0Ch. Since 0x0Ch is in the common space, Bit 6 and Bit 7 are meaningless

R4=01111100 points to the register 0x3C in Bank 1

R4[7]Bk1	R4[6]Bk0	RAM Bank #
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	–

R5 (Data Line I/O Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	D- or PS/2	D+ or PS/2

R5 [0] D+ line register or PS/2 clock interface register

R5 [1] D- line register or PS/2 data interface register

These two bits are both writable and readable when the MCU is operating in PS/2 mode. But in USB Mode, these two bits cannot be accessed.

R5 [2~7] General purpose registers

R6 (Port 6 I/O Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

R7 (Port 7 I/O Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70

R8 (Port 6 Wake-up Pin Selection Register) Default Value: (0B_1111_1111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/Wu67	/wu66	/Wu65	/Wu64	/Wu63	/Wu62	/Wu61	/Wu60

R8 [0 ~ 7] Select which of the Port 6 pins are to be defined to wake up the MCU from sleep mode. When the state of the selected pins changes during sleep mode, the MCU will wake up and automatically execute the next instruction.

“0” : Enable wake-up function

“1” : Disable wake-up function

R9 (Port 7 Wake-up Pin Selection Register) Default Value: (0B_1111_1111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/Wu77	/Wu76	/Wu76	/Wu74	/Wu73	/Wu72	/Wu71	/Wu70

R9 [0~7] Select which of the Port 7 pins are to be defined to wake-up the MCU from sleep mode. When the state of the selected pins changes during sleep mode, the MCU will wake-up and execute the next instruction automatically.

“0” : Enable wake-up function

“1” : Disable wake-up function



RA (High Pattern Counter Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HP.7	HP.6	HP.5	HP.4	HP.3	HP.2	HP.1	HP.0

This register is used in pattern detecting application. If this function is disabled (IOCE[2] = 0), the PDA function is disabled. RA register is also used as a general-purpose register.

RB (Low Pattern Counter Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LP.7	LP.6	LP.5	LP.4	LP.3	LP.2	LP.1	LP.0

This register is used in pattern detecting application. If this function is disabled (IOCE[2] = 0), the PDA function is disabled. RB register is also used as a general-purpose register.

RC (USB Application Status Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EP0_W	EP0_R	EP1_R	-	Device_Resume	Host_Suspend	EP0_Busy	Stall

- RC [0] Stall flag. When the MCU receives an unsupported command or invalid parameters from host, this bit will be set to 1 by the firmware to notify the UDC to return a STALL handshake. When a successful setup transaction is received, this bit is cleared automatically. This bit is both readable and writable.
- RC [1] EP0 Busy flag. When this bit is equal to “1,” it indicates that the UDC is writing data into the EP0’s FIFO or reading data from it. During this time, the firmware will avoid accessing the FIFO until the UDC finishes writing or reading. This bit is only readable.
- RC [2] Host Suspend flag. If this bit is equal to 1, it indicates that the USB bus has no traffic for a specified period of 3.0 ms. This bit will also be cleared automatically when a bus activity takes place. This bit is only readable.
- RC [3] Device Resume flag. This bit is set by firmware to generate a signal to wake up the USB host and is cleared as soon as the USB Suspend signal becomes low. This bit can only be set by firmware and cleared by hardware.
- RC [4] Undefined Register. The default value is 0.
- RC [5, 6] EP0_R / EP1_R flag. These two bits inform the UDC to read the data written by firmware from the FIFO. Then the UDC sends the data to the host automatically. After UDC the finishes reading the data from the FIFO, this bit is cleared automatically.

Thus, before writing data into the FIFO, the firmware will first check this bit to prevent overwriting the existing data. These two bits can only be set by firmware and cleared by hardware.

RC [7] EP0_W flag. After the UDC completes writing data to the FIFO, this bit will be set automatically. The firmware will clear it as soon as it gets the data from EP0's FIFO. Only when this bit is cleared that the UDC will be able to write a new data into the FIFO.

Hence, before the firmware can write a data into the FIFO, this bit must first be set by the firmware to prevent the UDC from writing data at the same time. This bit is both readable and writable.

RD (USB Application FIFO Address Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	UAD4	UAD3	UAD2	UAD1	UAD0

RD [0~4] USB Application FIFO address registers. These five bits are the address pointer of USB Application FIFO.

RD [5~7] Undefined registers. The default value is zero.

RE (USB Application FIFO Data Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UD7	UD6	UD5	UD4	UD3	UD2	UD1	UD0

RE (USB Application FIFO data register) contains the data in the register of which address is pointed by RD.

RF (Interrupt Status Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Low Signal_IF	High Signal_IF	Port 5 State Change_IF	USB Host Resume_IF	USB Reset_IF	USB Suspend_IF	EP0_IF	TCC_IF

RF [0] TCC Overflow interrupt flag. It will be set while TCC overflows, and is cleared by the firmware.

RF [1] EndPoint Zero interrupt flag. It will be set when the EM78M612 receives Vendor/Customer Command to EndPoint Zero. This bit is cleared by the firmware.

RF [2] USB Suspend interrupt flag. It will be set when the EM78M612 finds the USB Suspend Signal on USB bus. This bit is cleared by the firmware.

RF [3] USB Reset interrupt flag. It will be set when the host issues the USB Reset signal.

RF [4] USB Host Resume interrupt flag. It is set only in Dual Clock mode when the USB suspend signal becomes low.

RF [5] Port 5 State Change interrupt flag. It is set when the Port 5 state changes.

RF [6, 7] High/Low signal Counter Interrupt flag. These two flags are used for pattern detecting application.

R10~R1F are General purpose registers. These registers can be used no matter what Bank Selector is. There are three banks (BK0 ~ BK2) **R20~R3F** General purpose registers, selected by R4 [6, 7].

5.2.1.2 Operation Registers in Bank 1

The special purpose registers for special operation (R8S~RES), are located in Special Purpose Register Bank 1. To access these registers, bank selector (R3 [7]) must be set first. These Bank 1 located registers serve special functions, such as; E²PROM, Pulse Width Modulation, and Analog to Digital Converter. These registers and the above mentioned special functions are described in details in Sections 8.2.3, 8.9, and 8.10 respectively in this specification.

R8S (PWM1 Duty Cycle Register) Default Value: (0B_0000_0000)

A specified value keeps the output of PWM1 remain at high for a period of time.

R9S (PWM2 Duty Cycle Register) Default Value: (0B_0000_0000)

A specified value keeps the output of PWM2 remain at high for a period of time.

RAS (AD Channel Select Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC	Token_Bit	-	AD4	AD3	AD2	AD1	AD0

RAS [0]~[4]:AD Channel Selector

AD4	AD3	AD2	AD1	AD0	Channel	Input Port
0	0	0	0	0	Disable AD	-
0	0	0	0	1	1	Reserved
0	0	0	1	0	2	P61
0	0	0	1	1	3	P62
0	0	1	0	0	4	P63
0	0	1	0	1	5	P64
0	0	1	1	0	6	P65
0	0	1	1	1	7	P66
0	1	0	0	0	8	P67
0	1	0	0	1	9	P70
0	1	0	1	0	10	P71
0	1	0	1	1	11	P72
0	1	1	0	0	12	P73
0	1	1	0	1	13	P74
0	1	1	1	0	14	P75
0	1	1	1	1	15	P76
1	0	0	0	0	16	P77

RAS [6] Token_Bit will be latched to high by hardware when the USB bus is transferring token packet. This bit is reset by firmware only.

RAS [7] AD Converter ready flag

0 → 1 : Start AD Conversion. (Bit set by Firmware)

1 → 0 : When AD Conversion is finished and digital data is moved into the AD Data Register, this bit is cleared by hardware.

NOTE

This function is enabled by hardware only at the AD Channel Selector on the functional I/O port.

RBS (AD MSB Data Register). This register is Read only.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2

RCS (AD LSB Data Register). This register is Read only.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 1	Bit 0	-	-	-	-	-	-

RES (EEPROM Mode Select Register) Default Value (0B_1111_1111)

Command Value	Action	Execution Time
0B_0000_0000	Read	1ms
0B_0000_0001	Write	9ms
0B_0000_0010	Erase	128ms
0B_0000_0011	Disable	N.A.

5.2.1.3 Control Registers in Bank 0

Special purpose registers for special control purposes are also available. Except for the Accumulator (A), these registers must be read and written by special instructions. One of these registers, CONT, can only be read by the instruction "CONTR" and written by "CONTW" instruction. The remaining special control registers can be read by the instruction "IOR" and written by the instruction "IOW."

The following paragraphs only describe the general functions of the control registers. For more detailed description, refer to Sections 8.8 to 8.10 of this spec.



A (Accumulator Register)

The accumulator is an 8-bit register that holds operands and results of arithmetic calculations. It is not addressable.

CONT (Control Register) Default Value: (0B_0011_1111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RWB	/INT	TSR2	TSR1	TSR0	PSR2	PSR1	PSR0

The CONT register can be read by the instruction “CONTR” and written by the instruction “CONTW”.

CONT [0~2] Watchdog Timer prescaler bits. These three bits are used as the prescaler of the Watchdog Timer.

CONT [3~5] TCC Timer prescaler bits.

The relationship between the prescaler value and these bits are shown below:

PSR2/TSR2	PSR1/TSR1	PSR0/TSR0	TCC Rate	WDT Rate
0	0	0	1: 2	1: 1
0	0	1	1: 4	1: 2
0	1	0	1: 8	1: 4
0	1	1	1: 16	1: 8
1	0	0	1: 32	1: 16
1	0	1	1: 64	1: 32
1	1	0	1: 128	1: 64
1	1	1	1: 256	1: 128

Watchdog Timer :

WDT Rate	POT=500 μs	POT=2 ms	POT=8 ms	POT=16 ms
1: 1	500 μs	2 ms	8 ms	16 ms
1: 2	1 ms	4 ms	16 ms	32 ms
1: 4	2 ms	8 ms	32 ms	64 ms
1: 8	4 ms	16 ms	64 ms	128 ms
1: 16	8 ms	32 ms	128 ms	256 ms
1: 32	16 ms	64 ms	256 ms	512 ms
1: 64	32 ms	128 ms	512 ms	1024 ms
1: 128	64 ms	256 ms	1024 ms	2048 ms

CONT [6] Interrupt enable control bit. This bit toggles enable or disable the Interrupt function. It is set to 1 by the interrupt disable instruction "DISI" and reset by the interrupt enable instructions "ENI" or "RETI."

“0” : Enable Interrupt function

“1” : Disable Interrupt function

CONT [7] Remote Wake-up Bit. (Read only)

Tie to UDC Remote wake-up bit

“0” : Does Not Support

“1” : Support Remote Wakeup

IOC5 ~IOC7 (I/O Port [Port 5 ~ Port 7] Direction Control Registers)

Each bit controls the I/O direction of three I/O ports respectively. When these bits are set to 1, the relative I/O pins become input pins. Similarly, the I/O pins becomes outputs when the relative control bits are cleared.

“0” : Output direction

“1” : Input direction

IOC5 (Data Line I/O Control Register) Default Value: (0B_0000_0011)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	I/O	I/O

IOC5 [2~7] Undefined registers. The default value is 0.

IOC6 (Port 6 I/O Control Register) Default Value: (0B_1111_1111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	-

IOC6 [0] Undefined register. This is because P60 can only be used as an input pin.

IOC7 (Port 7 I/O Control Register) Default Value: (0B_1111_1111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70

IOC8 (Sink Current Control Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	Sink1.1	Sink1.0	-	-	Sink0.1	Sink0.0

IOC8 [0, 1] [4, 5] are P70/P71 sink current control registers. Four levels are offered for selection:

Sink0.1/1.1	Sink0.0/1.0	Sink Current
0	0	3 mA \pm 10%
0	1	6 mA \pm 10%
1	0	12 mA \pm 10%
1	1	30 mA \pm 10%

The default current after Power-on reset is 3mA.

IOC9 (Pattern Detecting Application Control Register) Default Value: (0B_0111_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	Sample Time.2	Sample Time.1	Sample Time.0	-	DB.2	DB.1	DB.0

IOC9 [0~2] Debounce control registers. This is used for Pattern Detecting Application. There are seven degrees available to debounce the input signal noise.

IOC9 [4~6] Sample time selection registers. This is used for Pattern Detecting Application. The default value is 111.

Sample Time.2	Sample Time.1	Sample Time.0	Sample Time
0	0	0	1/(6 MHz or 12 MHz)
0	0	1	$[1/(6 \text{ MHz or } 12 \text{ MHz})] \times 2$
0	1	0	$[1/(6 \text{ MHz or } 12 \text{ MHz})] \times 4$
0	1	1	$[1/(6 \text{ MHz or } 12 \text{ MHz})] \times 8$
1	0	0	$[1/(6 \text{ MHz or } 12 \text{ MHz})] \times 16$
1	0	1	$[1/(6 \text{ MHz or } 12 \text{ MHz})] \times 32$
1	1	0	$[1/(6 \text{ MHz or } 12 \text{ MHz})] \times 64$
1	1	1	$[1/(6 \text{ MHz or } 12 \text{ MHz})] \times 128$

Debounce Time.2	Debounce Time.1	Debounce Time.0	Debounce Time
0	0	0	0
0	0	1	Sample Time
0	1	0	Sample Time \times 2
0	1	1	Sample Time \times 3
1	0	0	Sample Time \times 4
1	0	1	Sample Time \times 5
1	1	0	Sample Time \times 6
1	1	1	Sample Time \times 7

IOC9 [3 and 7] Undefined registers. The default value is Zero.

IOCA (Operation Mode Control Register) Default Value: (0B_1100_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Dual_Frq.1	Dual_Frq.0	-	-	-	-	PS/2	USB

IOCA [0, 1] These two bits are used to select the operation mode. EM78M612 can auto-detect the type of port device being attached. After identifying the port, the firmware will set these two bits to enter into a proper operation mode. The definition of these two control registers is described in the table below.

IOCA[1]	IOCA[0]	Operation Mode
0	0	Detect Mode
0	1	USB Mode
1	0	PS/2 Mode
1	1	USB Test Mode

IOCA [2~5] Undefined registers. The default value is 0.

IOCA [6, 7] Select the operation frequency in Dual Clock mode. Four frequencies are available and can be chosen as Dual Clock mode for running the MCU program.

Dual_Frq.1	Dual_Frq.0	Frequency
0	0	500Hz
0	1	4kHz
1	0	32kHz
1	1	256kHz

IOCB (Port 6 Pull-low Control Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	-

IOCB [0] Undefined register. P60 is always without pull-low resistor.

IOCB [1~7] Select whether the 15 K Ω pull-low resistor of Port 6 individual pin is connected or not.

“0” : Disable pull-low function

“1” : Enable pull-low function

IOCC (Port 6 Pull-high Control Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	-

IOCC [0] Undefined register. P60 is always without pull-high resistor.



IOCC [1~7] Select whether the 200 KΩ pull-high resistor of Port 6 individual pin is connected or not.

“0” : Disable pull-high function

“1” : Enable pull-high function

IOCD (Port 7 Pull-High Control Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70

IOCD [0~7] Select whether the 200 KΩ pull-high resistor of Port 7 individual pin is connected or not.

“0” : Disable pull-high function

“1” : Enable pull-high function

IOCE (Special Function Control Register) Default Value: (0B_1111_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/Dual clock	/WUE	WTE	RUN	-	PDA	-	-

IOCE [2] Pattern Detecting Application Enable Bit. This bit enables the Pattern Detecting function which is used in Serial Signal Transmission. When this feature is enabled, P60 becomes a serial input pin allowing one pattern detecting block, a counter, and two comparators to function.

“0” : Disable Pattern Detecting function

“1” : Enable Pattern Detecting function

IOCE [3] Undefined register. The default value is zero.

IOCE [4] Run bit. This bit can be cleared by the firmware and set during power-on, or by the hardware at the falling edge of wake-up signal. When this bit is cleared, the clock system is disabled and the MCU enters into power down mode. At the transition of wake-up signal from high to low, this bit is set to enable the clock system.

“0” : Sleep mode. The EM78M612 is in power down mode.

“1” : Run mode. The EM78M612 is working normally.

IOCE [5] Watchdog Timer enable bit. This bit disables/enables the Watchdog Timer.

“0” : Disable WDT

“1” : Enable WDT

IOCE [6] Enable the wake-up function as triggered by port-change. This bit is set by the UDC.

“0” : Enable wake-up function

“1” : Disable wake-up function

IOCE [7] Dual Clock Control bit. This bit is used to select the frequency of the system clock. When this bit is cleared, the MCU will run on very low frequency to save power and the UDC will stop working.

“0” : Run on slow frequency

“1” : Run on normal frequency

IOCF (Interrupt Mask Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Low Signal_IE	High Signal_IE	Port 5 State Change_IE	USB Host Resume_IE	USB Reset_IE	USB Suspend_IE	EP0_IE	TCC_IE

IOCF [0~7] TCC / EP0 / USB Suspend / USB Reset / USB Host Resume / Port 5 State Change / High Signal / Low Signal interrupt enable bits. These eight bits respectively control the function of the TCC interrupt, EP0 interrupt, USB Suspend interrupt, USB Reset interrupt, USB Host Resume interrupt, Port 5 State Change interrupt, High pattern counter interrupt and Low pattern counter interrupt. Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

“0” : Disable Interrupt

“1” : Enable Interrupt

Only when the global interrupt is enabled by the ENI instruction that the individual interrupts will work. After DISI instruction, any interrupt will not work even if the respective control bits of IOCF are set to 1.

The USB Host Resume Interrupt works only under Dual clock mode. This is because when the MCU is in sleep mode, it will be woken up automatically by the UDC Resume signal.

5.2.1.4 Control Registers in Bank 1

Bank 1 has more special purpose control registers. To write or read these registers, the bank selector (R3 [7]) must be initially set to 1. For more detailed description of these registers, refer to Sections 8.8 to 8.10 of this spec.

IOC8S (PWM Control Register) Default Value : (0B_0000_0111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PEN2	PEN1	-	-	-	PS2	PS1	PS0

IOC8S [0~2] PWM Frequency and Prescaler

PS2	PS1	PS0	PWM @OSC = 6 MHz	PWM @OSC = 12 MHz
			Frequency / Prescaler	Frequency / Prescaler
0	0	0	7.84kHz / 0.5μs	15.69kHz / 0.25μs
0	0	1	3.92kHz / 1μs	7.84kHz / 0.5μs
0	1	0	1.96kHz / 2μs	3.92kHz / 1μs
0	1	1	980Hz / 4μs	1.96kHz / 2μs
1	0	0	490Hz / 8μs	980Hz / 4μs
1	0	1	245Hz / 16μs	490Hz / 8μs
1	1	0	122.5Hz / 32μs	245Hz / 16μs
1	1	1	61.25Hz / 64μs	122.5Hz / 32μs

IOC8S [6] PWM1 (P64) Enable Bit

“0” : Disable

“1” : Enable

IOC8S [7] PWM2 (P65) Enable Bit

“0” : Disable

“1” : Enable

IOCAS (AD Control Register) Default Value : (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	ADPS1	ADPS0

IOCAS [0, 1]: AD Clock Prescaler

ADPS1	ADPS0	AD Clock Source	Conversion Rate
0	0	RC	20kHz
0	1	RC/2	10kHz
1	0	RC/4	5kHz
1	1	RC/8	2.5kHz

RC = 256kHz

5.2.2 USB Application FIFOs

For USB Application, the EM78M612 provides an 8-bit First-In-First-Out (FIFO) buffer for each endpoint. The buffer cannot be accessed directly. However, a corresponding Data Byte Pointer register for each endpoint is made available to address the individual byte of the FIFO buffer. The contents of the individual byte will be mapped to a special register.

5.3 I/O Ports

The EM78M612 has 15 General Purpose I/O pins, which are classified into two port groups; Port 6 and Port 7. Each pin has an internal resistor that can be individually selected by user. Notice that P60 is an input only pin.

The following describes the important features of the EM78M612 I/O pins.

5.3.1 Programmable Large Current

Port 7 has two pins; P70 and P71 that can drive large currents of up to 30 mA. The range of driving current is from 3mA to 30mA, which is programmable. Use IOC8 [0, 1] and IOC8 [4,5] to control the sink current of P70/P71. The default sink current is 3 mA.

5.3.2 Wake up by Port Change Function

Each of the GPIO pins in Port 6 and Port 7 can wake up the MCU through signal change from the input pin. This function is used to automatically wake up the MCU from sleep mode. It also supports the remote wake-up function for USB application.

Any of the Individual pins of Port 6 and Port 7 can be defined to wake up the MCU by setting their respective bits, R8 and R9.

5.4 USB Application

The EM78M612 is specially designed for USB device application and has many powerful functions that help the firmware to free itself from complex situation in various aspects of USB application.

5.4.1 Auto-Detect PS/2 or USB Mode

When the EM78M612 is connected to the bus, it will auto-detect and identify which type of bus (USB or PS/2) it is connected to. The conditions that influence auto-detect function are described below:

1. After a Power-on reset, the initial value of IOCA [0, 1] is 0b00. Thus the operation mode is "Detect mode" and the D+ and D- I/O pins are internally pulled high by the 200 K Ω to VDD.
2. The firmware checks the state of R5 [0, 1]. If the state with which these two bits are 0b00, set the IOCA [0] to "1" to indicate "USB mode." Otherwise, set the IOCA [1] to "1," to indicate "PS/2 mode."
3. When the operation mode is defined as "USB mode," the D- I/O pin is internally pulled high by a 1.5 K Ω resistor to 3.3V, which is output from a built-in regulator.
4. If the operation mode is in "PS/2 mode," both of the PS/2 interface I/O pins are internally pulled high by a 2.2 K Ω resistor to VDD.



NOTE

If the auto-detect function is not used, the firmware should set the operation mode at the beginning of the program, either in USB mode or PS/2 mode.

An additional mode, “USB Test Mode” is also available. This mode has no load on D+ and D- I/O pins, and can only be used in USB Application case. Therefore, an external 1.5 K Ω resistor is needed to pull up the D- I/O pin to 3.3V.

In “PS/2 mode,” both PS/2 pins are programmed to generate an interrupt. After setting the Port 5 State change to Interrupt Enable bit, an MCU interrupt will occur while the state of these two pins changes.

5.4.2 USB Device Controller

The USB Device Controller (UDC) built-in in the EM78M612 can interpret the USB Standard Command and respond automatically without involving the firmware. The embedded Serial Interface Engine (SIE) handles the serialization and de-serialization of actual USB transmission. Thus, a designer can concentrate his efforts more in perfecting the device actual functions and spend less effort in dealing with USB transactions.

The UDC handles and decodes most Standard USB commands defined in the USB Specification Rev1.1. If the UDC receives an unsupported command, it will set a flag to notify the MCU of the receipt of such command. The Standard Commands that the EM78M612 supports includes; Clear Feature, Get Configuration, Get Interface, Get Status, Set Address, Set Configuration, Set Feature, and Set Interface.

Each time the UDC receives a USB command, it writes the command into the EP0’s FIFO. Only when it receives unsupported commands will the UDC notify the MCU through an interrupt.

This feature makes the EM78M612 very flexible for USB applications since the designer can freely choose the method of decoding the USB commands as per what different situations require.

5.4.3 Device Address and Endpoints

The EM78M612 supports one device address, two endpoints, EP0 for control endpoint, and EP1 for interrupt endpoint. Sending data to the USB host in the EM78M612 is very easy. Just write data into the EP’s FIFO, set the flag, and the UDC will handle the rest. It will then confirm that the USB host has received the correct data from the EM78M612.

5.5 Reset

The EM78M612 provides three types of reset: (1) Power-on Reset, (2) Watchdog Reset, and (3) USB Reset.

5.5.1 Power-on Reset

Power-on Reset occurs when the device is attached to power and a reset signal is initiated. The signal will last until the MCU becomes stable. After a Power-on Reset, the MCU enters into the following predetermined states (see below), and then, it is ready to execute the program.

1. The program counter is cleared.
2. The TCC timer and Watchdog timer are cleared.
3. Special registers and Special Control registers are all set to their initial values.

The MCU also has a low voltage detector that detects low output power condition. Whenever the output voltage of the 3.3V regulator decreases to below 2.2V, a reset signal is set off.

5.5.2 Watchdog Reset

When the Watchdog timer overflows, it causes the Watchdog to reset. After it resets, the program is executed from the beginning and some registers will be reset. The UDC however, remains unaffected.

5.5.3 USB Reset

When UDC detects a USB Reset signal on the USB Bus, it interrupts the MCU, then proceed to perform the specified process that follows.

5.6 Power Saving Mode

The EM78M612 provides two options of power saving modes for energy conservation, i.e., Power Down mode, and Dual Clock mode.

5.6.1 Power-down Mode

The EM78M612 enters into Power Down mode by clearing the RUN register (IOCE[4]). During this mode, the oscillator is turned off and the MCU goes to sleep. It will wake up when signal from USB host is resumed, or when the Watchdog resets, or the input port state changes.

If the MCU wakes up when the I/O port status changes, I/O port direction should be set at input, then the port state is read. For example:

```
:  
// Set the Port 6 to input port  
MOV      A,@0XFF  
IOW      PORT6  
// Read the state of Port 6  
MOV      PORT6,PORT6  
// Clear the RUN bit  
IOR      0X0E  
AND      A,@0B11101111  
IOW      0X0E  
:  
:
```

5.6.2 Dual Clock Mode

The EM78M612 has one internal oscillator for power saving application. Clearing the Bit IOCE [7] will enable the low frequency oscillator. At the same time, the external oscillator will be turned off. Then the MCU will run under very low frequency to conserve power. Four types of frequency are available for selection in setting Bits IOCA [6, 7].

The USB Host Resume Interrupt can only be used in this mode. If this interrupt is enabled, the MCU will be interrupted when the USB Suspend signal is detected on the USB Bus.

5.7 Interrupt

The EM78M612 has two interrupt vectors, one is in 0x0001, and the other is in 0x000A. When an interrupt occurs while the MCU is running, it will jump to the interrupt vector (0x0001 or 0x000A) and execute the instructions sequentially from the interrupt vector. RF is the interrupt status register that records the interrupt status in the relative flags/bits.

The interrupt condition could be one of the following:

- TCC Overflow When the Timer Clock / Counter Register (R1) overflows, the status flag RF[0] will be set to 1. Its interrupt vector is 0x0001.
- EP0 Interrupt When the UDC successfully received a setup transaction from host to EndPoint0, the status flag RF[1] will be set to 1. Its interrupt vector is 0X000A.
- USB Suspend When UDC detects a USB Suspend signal on USB bus, the status flag RF[2] will be set to 1. Its Interrupt Vector is 0x000A.



- USB Reset When the UDC detects a USB Reset signal on the USB bus, the status flag R [3] will be set to 1. Its Interrupt Vector is 0x000A.
- USB Host Resume When the UDC detects that the USB bus has left the Suspend condition, the status flag R [4] will be set to 1. Its Interrupt Vector is 0x000A.
- Port 5 State Change When the input signal in Port 5 changes, the status flag RF [5] will be set to 1. Its Interrupt Vector is 0x0001.
- High Pattern Detecting Interrupt Conditions If the Pattern Detecting Application function is enabled, there will be three conditions with which an interrupt is generated, and the status flag RF [6] is set to 1. The Interrupt Vector is 0x0001.
 - P.60 turns to low, and the Pattern Counter value is bigger than the RA register value.
 - P.60 remains at high, and the Pattern Counter value is 0xFF.
 - Pattern Counter value is bigger than 0xFF and P.60 turns to low.
- Low Pattern Counter Interrupt Conditions. If the function is enabled, there will be three conditions with which an interrupt is generated and the status flag RF [7] is set to 1. Its Interrupt Vector is 0x0001.
 - P.60 turns to high, and Pattern Counter value is bigger than RB register value.
 - P.60 remains low, and Pattern Counter value is 0xFF.
 - Pattern Counter value is bigger than 0xFF and P.60 turns to high.

IOCF is an interrupt mask register which can be set individually bit by bit. While their respective bit is written to 0, the hardware interrupt will be inhibited, that is, the EM78M612 will not jump to the interrupt vector to execute instructions. But the interrupt status flags still records the conditions no matter whether the interrupt is masked or not. The interrupt status flags must be cleared by firmware before leaving the interrupt service routine and enabling interrupt.

The global interrupt is enabled by the ENI (RETI) instruction and is disabled by the DISI instruction.



5.8 Pattern Detecting Application (PDA)

5.8.1 Function Description

This function is designed for the serial signal transmission, e.g., the transmission between a wireless device and its receiver box. The EM78M612 has a built-in Pattern Detecting Application block that ensures the EM78M612 supports wireless devices, such as receiver box controller for a wireless mouse.

Pattern Detecting Application (PDA) can calculate the length of one pattern and interrupt the MCU while the serial signal is transiting from high to low (or vice-versa). Then the MCU reads the length value from a specified register.

5.8.2 Control Register

RA (High Pattern Counter Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HP.7	HP.6	HP.5	HP.4	HP.3	HP.2	HP.1	HP.0

This register is used in pattern detecting application. If this function is disabled (IOCE[2] = 0), the PDA function is disabled. RA register is also used as a general-purpose register.

RB (Low Pattern Counter Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LP.7	LP.6	LP.5	LP.4	LP.3	LP.2	LP.1	LP.0

This register is used in pattern detecting application. If this function is disabled (IOCE[2] = 0), the PDA function is disabled. RB register is also used as a general-purpose register.

IOC9 (Pattern Detecting Application Control Register) Default Value: (0B_0111_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	Sample Time.2	Sample Time.1	Sample Time.0	-	DB.2	DB.1	DB.0

IOC9 [0~2] Debounce control registers. This is used for Pattern Detecting Application.

There are seven degrees available to debounce the input signal noise.

IOC9 [4~6] Sample time selection registers. This is used for Pattern Detecting Application. The default value is 111.



Sample Time.2	Sample Time.1	Sample Time.0	Sample Time
0	0	0	1/(6 MHz or 12 MHz)
0	0	1	[1/(6 MHz or 12 MHz)] × 2
0	1	0	[1/(6 MHz or 12 MHz)] × 4
0	1	1	[1/(6 MHz or 12 MHz)] × 8
1	0	0	[1/(6 MHz or 12 MHz)] × 16
1	0	1	[1/(6 MHz or 12 MHz)] × 32
1	1	0	[1/(6 MHz or 12 MHz)] × 64
1	1	1	[1/(6 MHz or 12 MHz)] × 128

Debounce Time.2	Debounce Time.1	Debounce Time.0	Debounce Time
0	0	0	0
0	0	1	Sample Time
0	1	0	Sample Time × 2
0	1	1	Sample Time × 3
1	0	0	Sample Time × 4
1	0	1	Sample Time × 5
1	1	0	Sample Time × 6
1	1	1	Sample Time × 7

IOC9 [3 and 7] Undefined register. The default value is Zero.

The PDA includes an enable control bit, an input pin (P60), a prescaler, a Pattern Detecting block, two special registers (RA and RB), and two interrupts (high pattern counter interrupt and low pattern counter interrupt).

To use this function, the enable control bit, IOCE[2] has to be set first. Otherwise the P60 will just be treated as an input only pin and the RA/RB as general purpose register.

As long as the IOCE[2] control bit is set to 1 and the P60 is set as input pin, the Pattern Detecting block will start to sample the P60 input signal and measure the high pulse or low pulse width. After detecting the transition of this signal and debounce, the value of the counter will be loaded into the RA (if the signal is transiting from high to low) or RB (if the signal is transiting from low to high), and the counter is cleared to start counting from zero.

Two interrupts are supported individually by RA and RB. After the PDA function is enabled (by setting IOCE[2] to 1), a default value is written to the High Pattern counter register and Low Pattern counter register. Then define the corresponding interrupt enable bits (IOCF[6] and IOCF[7]). When the counter value of one "H" pattern is bigger than the RA default value, then the High Pattern Detecting interrupt will be generated. Similarly, if the counter value of one "L" pattern is bigger than the RB default value, the Low Pattern Detecting interrupt will occur. Then, the EM78M612 will be notified that one successful pattern is received from P60.

If these two interrupts are not used, they can be masked. The new counter value of a pattern will still be loaded to the RA and RB. The firmware must be made to poll and determines any changes to the value of these two registers.

The sample clock is programmable with 8 frequencies to choose from.

*Note: For PDA application, refer to http://www.emc.com.tw/twn/tech_pc.asp

5.9 Pulse Width Modulation (PWM)

5.9.1 Function Description

In PWM mode, both of PWM1 (P64) and PWM2 (P65) produce up to a 8-bit resolution PWM output. PWM output has a duty cycle and keeps the output high.

The PWM Period is defined as $0xFF * (1/\text{Timer Counter Clock})$. The Timer Counter clock source is controlled by Control Register IOC8S. For example; if the Clock source is 1MHz, then the Period will be 255 μ seconds.

Period = 255 * (1/Timer Counter Clock)

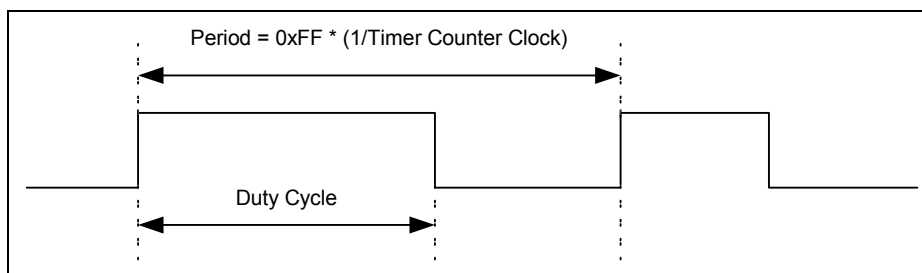


Figure 5-2 PWM Output Timing

IOC8S [0~2]

PS2	PS1	PS0	PWM Timer Counter Clock Source (Hz)
0	0	0	(6 MHz or 12 MHz) / 3
0	0	1	(6 MHz or 12 MHz) / 6
0	1	0	(6 MHz or 12 MHz) / 12
0	1	1	(6 MHz or 12 MHz) / 24
1	0	0	(6 MHz or 12 MHz) / 48
1	0	1	(6 MHz or 12 MHz) / 96
1	1	0	(6 MHz or 12 MHz) / 192
1	1	1	(6 MHz or 12 MHz) / 384

The PWM duty cycle is defined by writing to the R8S/R9S Register for PWM1/PWM2.

$$\text{Duty Cycle} = \frac{R8S}{255} \times 100\% \quad \text{for PMW1}$$

$$\text{Duty Cycle} = \frac{R9S}{255} \times 100\% \quad \text{for PMW2}$$

5.9.2 Control Register

R8S (PWM1 Duty Cycle Register)

A specified value keeps the output of PWM1 to remain at high within a period of time.

R9S (PWM2 Duty Cycle Register)

A specified value keeps the output of PWM2 to remain at high within a period of time.

IOC8S (PWM Control Register) Default Value: (0B_0000_0111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PEN2	PEN1	-	-	-	PS2	PS1	PS0

IOC8S [0~2] PWM Frequency and Prescaler

PS2	PS1	PS0	PWM @ OSC = 6 MHz	PWM @OSC = 12 MHz
			Frequency / Prescaler	Frequency / Prescaler
0	0	0	7.84kHz / 0.5μs	15.69kHz / 0.25μs
0	0	1	3.92kHz / 1μs	7.84kHz / 0.5μs
0	1	0	1.96kHz / 2μs	3.92kHz / 1μs
0	1	1	980Hz / 4μs	1.96kHz / 2μs
1	0	0	490Hz / 8μs	980Hz / 4μs
1	0	1	245Hz / 16μs	490Hz / 8μs
1	1	0	122.5Hz / 32μs	245Hz / 16μs
1	1	1	61.25Hz / 64μs	122.5Hz / 32μs

IOC8S [6, 7] PWM1/PWM2 Enable Bit

“0” : Disable

“1” : Enable

*Note: For PWM application, refer to http://www.emc.com.tw/twn/tech_pc.asp

5.10 Analog-to-Digital Converter (ADC)

5.10.1 Function Description

The Analog to Digital converter consists of a 5-bit analog multiplexer, one Control Register (IOCAS), one AD Channel Select Register (RAS), and two data registers (RBS and RCS) for 10-bit resolution

The ADC module utilizes successive approximation to convert the unknown analog signal to a digital value. The result is fed to the AD DATA. Input channels are selected by the analog input multiplexer via the ADCS/RAS bits AD0~AD4.

The reference pin must be connected to a voltage source capable of driving the reference input resistance which can be as low as 10 KΩ.

- 10-bit resolution: 0x00-00~0xC0-FF
- Internal Reference: V3.3 pin output voltage 3.0V ~ 3.6V
- Start (0x00-00): $0 \text{ Vref} \sim (1/1024) \times \text{Vref}$
- Full (0xC0-FF): $(1023/1024) \times \text{Vref} \sim \text{Vref}$
- Conversion Rate: 2.5K; 5K; 10K; and 20K

5.10.2 Control Register

RAS (AD Channel Select Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC	Token Bit	–	AD4	AD3	AD2	AD1	AD0

RAS [0~4]: AD Channel Selector

AD4	AD3	AD2	AD1	AD0	Channel	Input Port
0	0	0	0	0	Disable AD	–
0	0	0	0	1	1	Reserved
0	0	0	1	0	2	P61
0	0	0	1	1	3	P62
0	0	1	0	0	4	P63
0	0	1	0	1	5	P64
0	0	1	1	0	6	P65
0	0	1	1	1	7	P66
0	1	0	0	0	8	P67
0	1	0	0	1	9	P70
0	1	0	1	0	10	P71
0	1	0	1	1	11	P72
0	1	1	0	0	12	P73
0	1	1	0	1	13	P74
0	1	1	1	0	14	P75
0	1	1	1	1	15	P76
1	0	0	0	0	16	P77

RAS [6] Token Bit. This bit is asserted when the MCU receives or transmits USB transaction.

RAS [7] AD Converter ready flag

0 → 1: Start of AD Conversion (Set by firmware)

1 → 0 : When AD Conversion is finished and digital data is moved into the AD Data Register, this bit is cleared by hardware.

NOTE

The hardware can enable this function only at the AD Channel Selector of the functional I/O port. After Power-on reset, the initial value of this register is 0b0000 0000.

RBS (AD MSB Data Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2

8 bits AD Digital Data MSB.

RCS (AD LSB Data Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 1	Bit 0	-	-	-	-	-	-

AD Digital Data LSB 2 bits.

IOCAS (AD Control Register) Default Value: (0B_0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	ADPS1	ADPS0

IOCAS [0,1]:AD conversion clock source select.

00: 256kHz

01: 128kHz

10: 64kHz

11: 32kHz



5.11 EEPROM Application

5.11.1 Function Description

Four bytes of E²PROM are located in the IOCC ~ IOCF of Control Register Bank 1. The stored data of E²PROM are not erased when the power is off and can be read and rewritten by firmware. In some special case of applications, for example, cordless mouse controller, E²PROM can store important data, such as the cordless mouse's device identification number.

A control register, RES (Address: 0x0E in Bank 1) controls the E²PROM, i.e., to read, write, or to erase the data from E²PROM. Writing a command into this register will execute an action to E²PROM. The command value is defined in the following table. Note that there is an execution time lapse for each command. Before writing the next command into the control register, allow enough time for the E²PROM to finish processing the previous command.

5.11.2 Control Register

Command Value	Action	Execution Time
0B_0000_0000	Read	1 ms
0B_0000_0001	Write	9 ms
0B_0000_0010	Erase	128 ms
0B_0000_0011	Disable	N/A

*Note: For EEPROM application, refer to http://www.emc.com.tw/twn/tech_pc.asp

6 Absolute Maximum Ratings

Symbol	Min	Max	Unit
Temperature under bias	0	70	°C
Storage temperature	-65	150	°C
Input voltage	-0.5	6.0	V
Output voltage	-0.5	6.0	V

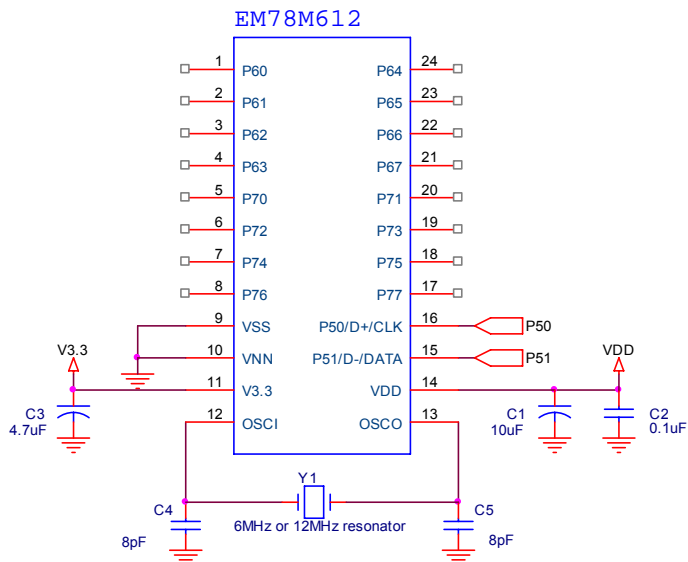
7 DC Electrical Characteristic

T = 25°C, VDD = 5V, VSS = 0V

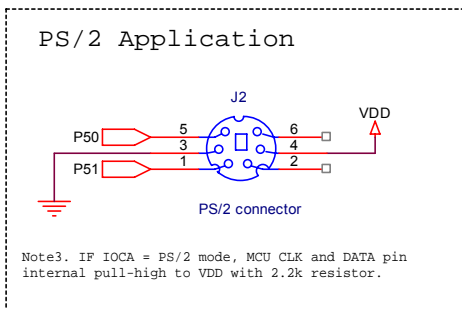
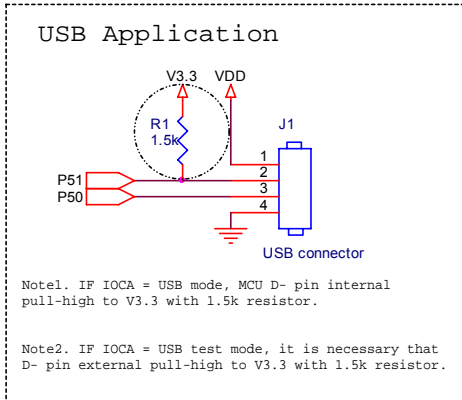
Symbol	Parameter	Condition	Min.	Type	Max.	Unit
3.3V Regulator						
V _{Reg}	Output voltage of 3.3V Regulator	VDD = 5.0V	3.0	3.3	3.6	V
V _{ResetL}	Low Power Reset detecting Low Voltage	-	-	-	2.2	V
V _{ResetH}	Low Power Reset detecting High Voltage	-	3.0	-	-	V
I _{Reg}	3.3V Regulator driving capacity	-	-	-	100	mA
MCU Operation						
VDD	Operating voltage	-	4.4	5.0	5.5	V
I _{IL}	Input Leakage Current for input pins	VIN= VDD, VSS	-	-	±1	μA
V _{IHX}	Clock Input High Voltage	OSCI	2.5	-	-	V
V _{ILX}	Clock Input Low Voltage	OSCI	-	-	1.0	V
I _{CC1}	VDD operating supply current – Normal frequency operation mode	Crystal type Freq. = 6 MHz Output pins floating	-	-	10	mA
I _{CC2}	VDD operating supply current – Normal frequency operation mode	Crystal type Freq. = 12MHz Output pins floating	-	-	20	mA
I _{SB1}	Operating supply current 1 – Power down mode	All input and I/O pins at VDD, Output pins floating WDT disabled	-	-	50	μA
I _{SB2}	Operating supply current 2 – Low frequency mode	RC oscillation type Freq. = 20kHz~50kHz Output pins floating	-	-	200	μA
GPIO Pins						
V _{IH}	Input High Voltage	-	2.0	-	-	V
V _{IL}	Input Low Voltage	-	-	-	0.8	V
V _{OH}	Output High Voltage (Port 5, Port 6 and P72~P77, OSCO)	I _{Drive} = 5.0mA	2.4	-	-	V
V _{OL}	Output Low Voltage (Port 5, Port 6 and P72~P77, OSCO)	I _{Sink} = 5.0mA	-	-	0.4	V
R _{PH}	Internal pull-high resistor	The input pin with internal pull-high resistor of Port 6 or Port 7 is connected to VReg.	-	200	-	KΩ
R _{PL}	Internal pull-low resistor	The input pin with internal pull-low resistor of Port 6 is connected to VSS.	-	15	-	KΩ

Symbol	Parameter	Condition	Min.	Type	Max.	Unit
USB Interface						
V_{OH}	Static Output High	USB operation Mode	2.8	-	3.6	V
V_{OL}	Static Output Low		-	-	0.3	V
V_{DI}	Differential Input Sensitivity		0.2	-	-	V
V_{CM}	Differential Input Command Mode Range		0.8	-	2.5	V
V_{SE}	Single Ended Receiver Threshold	USB operation Mode	0.8	-	2.0	V
C_{IN}	Transceiver Capacitance		-	-	20	pF
V_{RG}	Output Voltage of Internal Regulator		3.0	-	3.6	V
RD-	P51 (USB D-) Internal pull-high resistor		-	1.5	-	K Ω
Programmable Large Current						
I_{Sink1}	P70, P71 Output Sink Current	$V_{OUT} = 0.4V$, IOC8[0,1] or IOC8[4,5] = 00	-10%	3	+10%	mA
I_{Sink2}	P70, P71 Output Sink Current	$V_{OUT} = 0.4V$, IOC8[0,1] or IOC8[4,5] = 01	-10%	6	+10%	mA
I_{Sink3}	P70, P71 Output Sink Current	$V_{OUT} = 0.4V$, IOC8[0,1] or IOC8[4,5] = 10	-10%	12	+10%	mA
I_{Sink4}	P70, P71 Output Sink Current	$V_{OUT} = 0.4V$, IOC8[0,1] or IOC8[4,5] = 11	-10%	30	+10%	mA
Internal Memory Cycle Time						
TROM	Endurance of Program ROM	T = 25°C, Vpp=10V, VNN=-10V	1K	-	-	Cycle
TEE	Endurance of E2PROM	T = 25°C, VDD = 4.4V ~ 5.5V	4K	-	-	Cycle

8 Application Circuit



- Note :
- A. Place C1 and C2 close to MCU VDD pin.
 - B. Place Y1, C4 and C5 close to MCU OSCI pin.
 - C. In USB application, it is necessary to place C3 close to MCU V3.3 pin.
 - D. Port6 and Port7 are 3.3V level I/O.
 - E. Port60 is input only and without internal pull-high and pull-low resistor.



APPENDIX

A Special Registers Map

Operation Registers in Bank 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
0x00	R0	Indirect Addressing Register								0B_0000 _0000
0x01	R1 (TCC)	Timer/Clock Counter								0B_0000 _0000
0x02	R2 (PC)	Program Counter								0B_0000 _0000
0x03	R3 (STATUS)	SPRBS	-	PS0	T	P	Z	DC	C	0B_0001 _1000
0x04	R4 (RSR)	BK1	BK0	Select the register (Address: 00~3F) in indirect addressing mode						0B_0000 _0000
0x05	R5 (Port 5)	-	-	-	-	-	-	P51	P50	0B_0000 _0000
0x06	R6 (Port 6)	P67	P66	P65	P64	P63	P62	P61	P60	0B_0000 _0000
0x07	R7 (Port 7)	P77	P76	P75	P74	P73	P72	P71	P70	0B_0000 _0000
0x08	R8 (Port 8)	/Wu67	/Wu66	/Wu65	/Wu64	/Wu63	/Wu62	/Wu61	/Wu60	0B_1111 _1111
0x09	R9 (Port 9)	/Wu77	/Wu76	/Wu75	/Wu74	/Wu73	/Wu72	/Wu71	/Wu70	0B_1111 _1111
0x0A	RA	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	0B_0000 _0000
0x0B	RB	LP7	LP6	LP5	LP4	LP3	LP2	LP1	LP0	0B_0000 _0000
0x0C	RC	EP0_W	EP0_R	EP1_R	-	Device _Resume	Host _Suspend	EP0_Busy	STALL	0B_0000 _0000
0x0D	RD	USB Application FIFO Address Register								0B_0000 _0000
0x0E	RE	USB Application FIFO Data Register				-				0B_0000 _0000
0x0F	RF	Low Signal_IF	High Signal_IF	Port 5 State Change_IF	USB Host Resume_IF	USB Reset_IF	USB Suspend_IF	EP0_IF	TCC_IF	0B_0000 _0000



Control Registers in Bank 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
	CONT	RWB	/INT	TSR2	TSR1	TSR0	PSR2	PSR1	PSR0	0B_0111_1111
0x05	IOC5	-	-	-	-	-	-	P51	P50	0B_0000_0011
0x06	IOC6	P67	P66	P65	P64	P63	P62	P61	-	0B_1111_1111
0x07	IOC7	P77	P76	P75	P74	P73	P72	P71	P70	0B_1111_1111
0x08	IOC8	-	-	Sink1.1	Sink1.0	-	-	Sink0.1	Sink0.0	0B_0000_0000
0x09	IOC9	-	ST2	ST1	ST0	-	DB2	DB1	DB0	0B_0111_0000
0x0A	IOCA	Dual_Frq.1	Dual_Frq.0	-	-	-	-	PS/2	USB	0B_1100_0000
0x0B	IOCB	PL67	PL66	PL65	PL64	PL63	PL62	PL61	-	0B_0000_0000
0x0C	IOCC	PH67	PH66	PH65	PH64	PH63	PH62	PH61	-	0B_0000_0000
0x0D	IOCD	PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70	0B_0000_0000
0x0E	IOCE	/Dual clock	/WUE	WTE	RUN	-	PDA	-	-	0B_1111_0000
0x0F	IOCF	Low Signal_IE	High Signal_IE	Port 5 State change_IE	USB Host Resume_IE	USB Reset_IE	USB Suspend_IE	EP0_IE	TCC_IE	0B_0000_0000

*** One of these registers CONT, can only be read by the instruction "CONTR" and written by "CONTW" instruction. The other special control registers can be read by the instruction "IOR" and written by the instruction "IOW."

Operating Registers in Bank 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
0x08	R8S	PWM1 (P64) Duty Cycle Register								0B_0000_0000
0x09	R9S	PWM2 (P65) Duty Cycle Register								0B_0000_0000
0x0A	RAS	ADC	Token Bit	-	AD4	AD3	AD2	AD1	AD0	0B_0000_0000
0x0B	RBS	AD_DB9	AD_DB8	AD_DB7	AD_DB6	AD_DB5	AD_DB4	AD_DB3	AD_DB2	0B_0000_0000
0x0C	RCS	AD_DB1	AD_DB0	-	-	-	-	-	-	0B_0000_0000
0x0E	RES	-	-	-	-	-	-	EE_MS1	EE_MS0	0B_1111_1111

Control Registers in Bank 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
0x08	IOC8S	PEN2	PEN1	-	-	-	PS2	PS1	PS0	0B_0000_0111
0x0A	IOCAS	-	-	-	-	-	-	ADPS1	ADPS0	0B_0000_0000
0x0C	IOCCS	EEPROM Byte 1 Temp Register								0B_1111_1111
0x0D	IOCDS	EEPROM Byte 2 Temp Register								0B_1111_1111
0x0E	IOCES	EEPROM Byte 3 Temp Register								0B_1111_1111
0x0F	IOCFS	EEPROM Byte 4 Temp Register								0B_1111_1111

B Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. All instructions are executed within one single instruction cycle (consisting of 2 oscillator periods), unless the program counter is changed by-

- (a) Executing the instruction "MOV R2,A", "ADD R2,A", "TBL", or any other instructions that write to R2 (e.g. "SUB R2,A", "BS R2,6", "CLR R2", ...).
- (b) Execute CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) which were tested to be true.

Under these cases, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

- (1). Every bit of any register can be set, cleared, or tested directly.
- (2). The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value



Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None ¹
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None ¹
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z, C, DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None ²
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

Note: ¹ This instruction is applicable for IOCx only

² This instruction is not recommended for RE and RF operation

C Package Information

E M 7 8 M 6 1 2 D D P

M -- MTP Type ←

Function Type :

A -- without EEPROM and ADC ←

D -- with EEPROM and ADC

Pin Number and Package Type : ←

- AP - 16-pin PDIP (300 mil)
- AM - 16-pin SOP (150 mil)
- BP - 18-pin PDIP (300 mil)
- BM - 18-pin SOP (300 mil)
- CP - 20-pin PDIP (300 mil)
- CM - 20-pin SOP (300 mil)
- GM - 20-pin SSOP (150 mil)
- DP - 24-pin PDIP (600 mil)
- DK - 24-pin PDIP (300 mil)
- DM - 24-pin SOP (300 mil)
- HM - 24-pin SSOP (150 mil)
- AW - 32-pin QFN (5*5*0.8mm)

Date Code

0 4 2 2 L

→ IC Version :

K – Version A

L – Version B

→ Week#

→ Year#

D Code Option

Option Byte 1

Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID_7	ID_6	ID_5	ID_4	ID_3	ID_2	ID_1	ID_0	/AD_HOLD	OST_1	OST_0	Frequency	/Protect

Bit 0 : /Protect bit

0 : Enable

1 : Disable

Bit 1: Frequency selection

0 : 12 MHz

1 : 6 MHz

Bits 2~3: OST <1:0> : Oscillator start-up timer

00 : 500 μ s

01 : 2 ms

10 : 8 ms

11 : 16 ms

Bit 4: /AD_HOLD : ADC hold option bit

0 : Enable

1 : Disable

Bits 5~12: ID <7:0> : User ID

Option Byte 2

Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	-	-	RS	-	Package_1	Package_0

Bits 0~1: Package <1:0> Package type selection

00 : 16 pins

01 : 18 pins

10 : 20 pins

11 : 24 pins

Bit 2: Reserved

Bit 3: RS : RS enable of transceiver

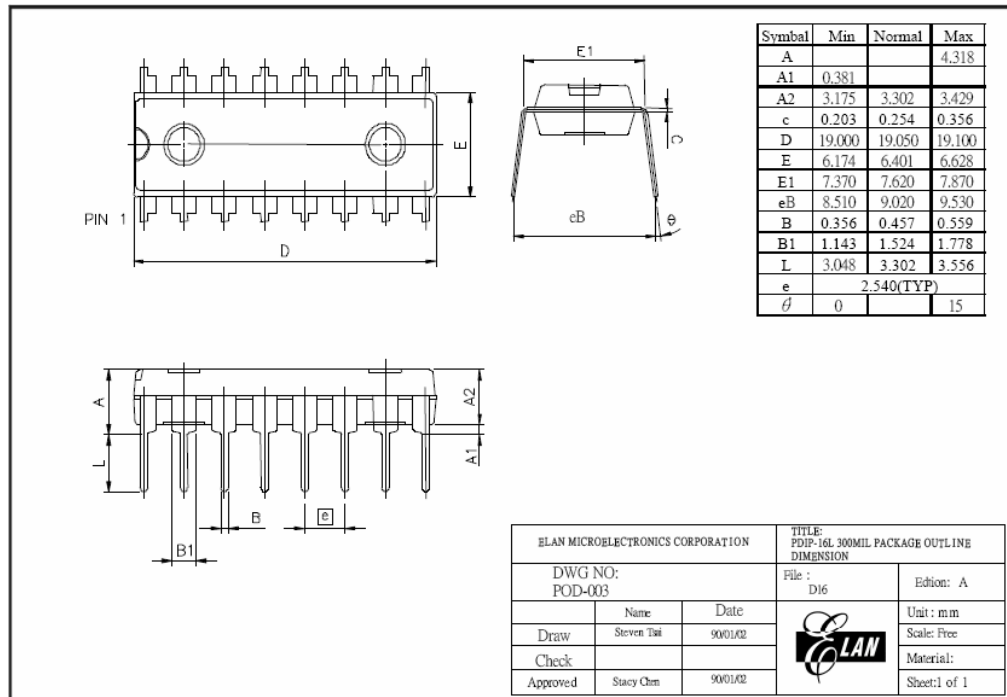
0 : Disconnect P51 (D-) pull-high resistor

1 : Connect P51 (D-) pull-high resistor

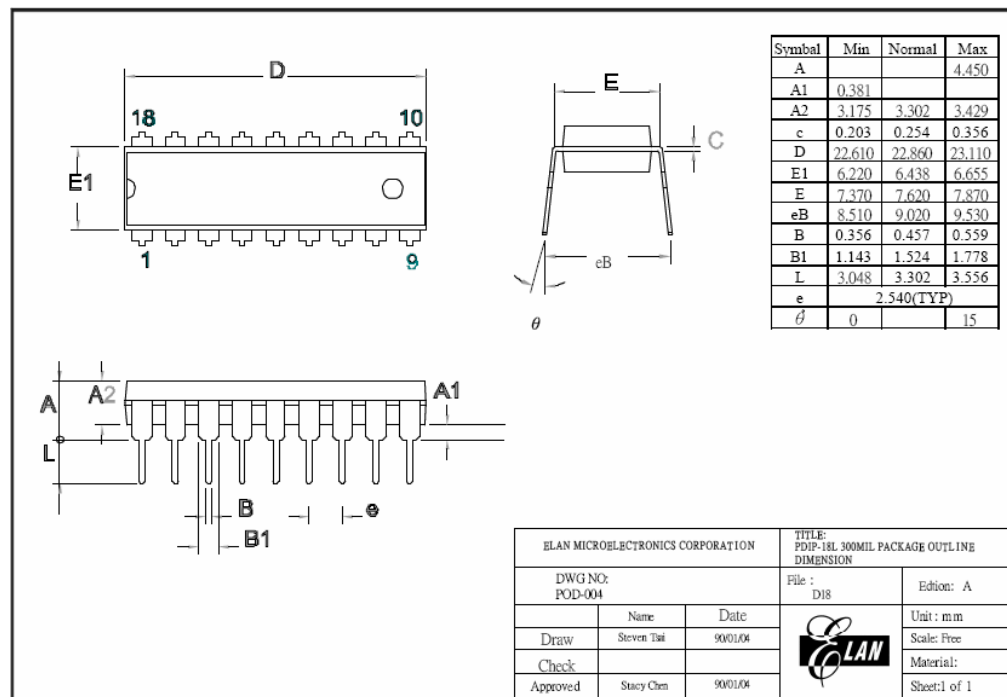
Bits 4~12: :Reserved

E Package Outline Dimension

EM78M612AAP and EM78M612DAP

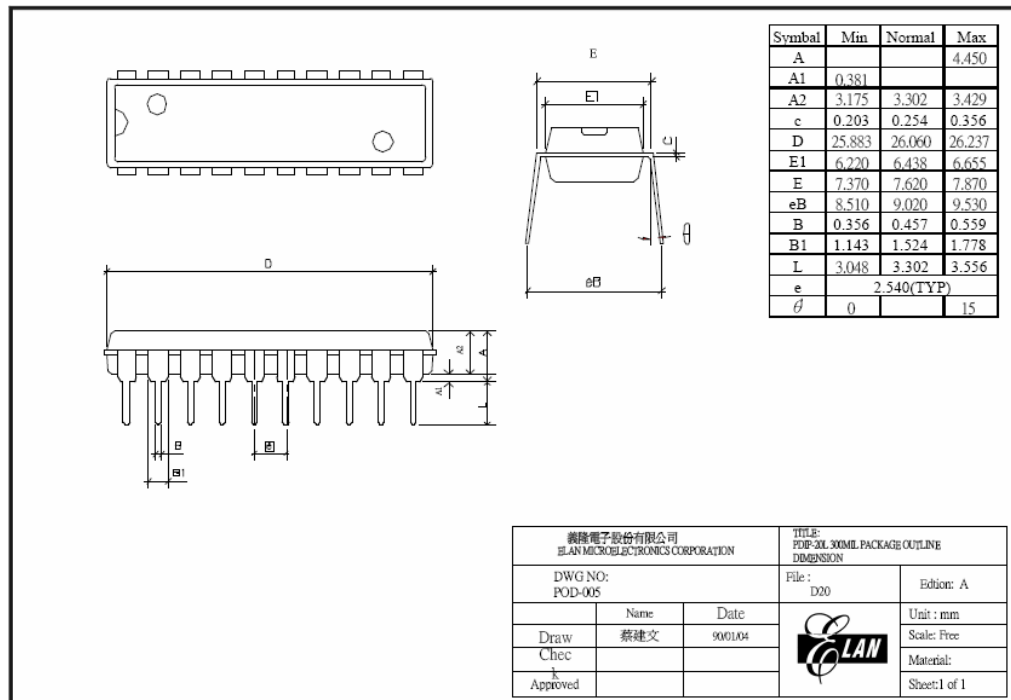


EM78M612ABP and EM78M612DBP

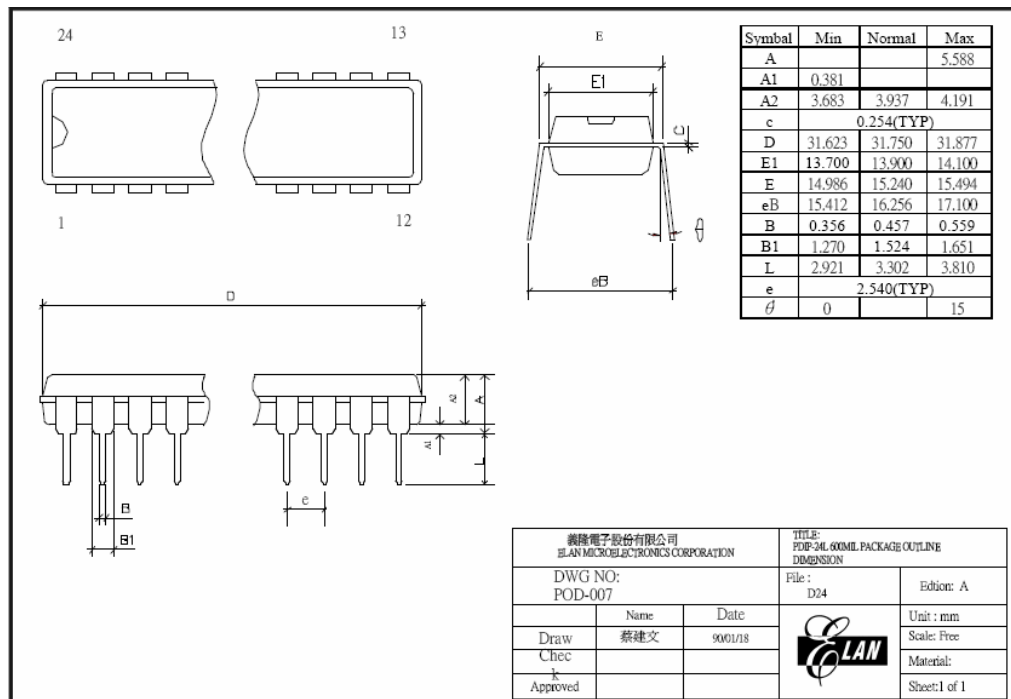




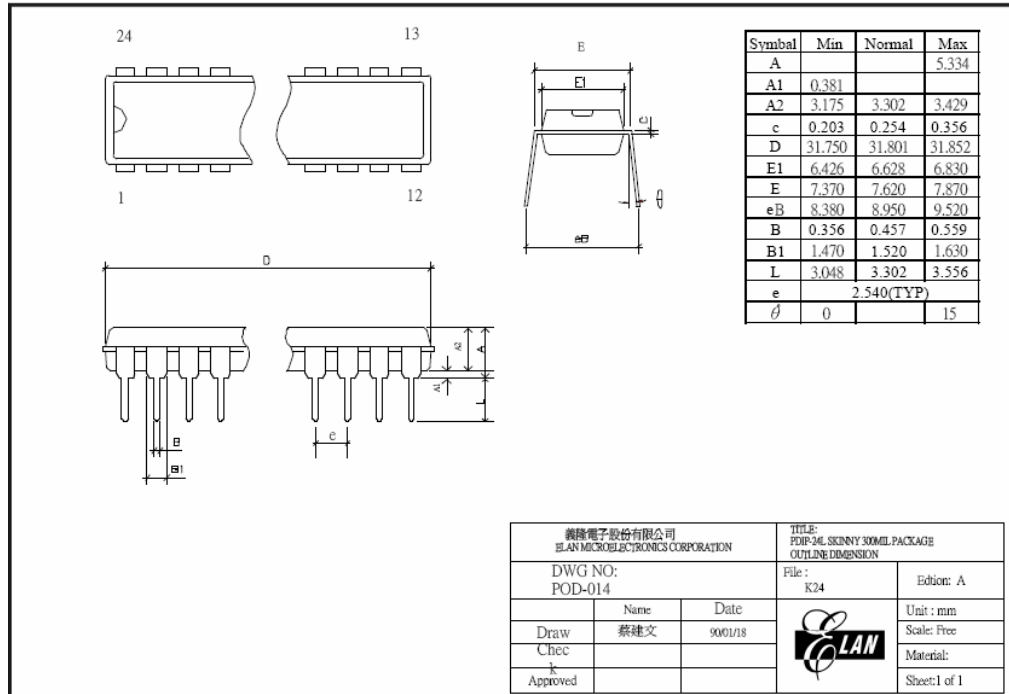
EM78M612ACP and EM78M612DCP



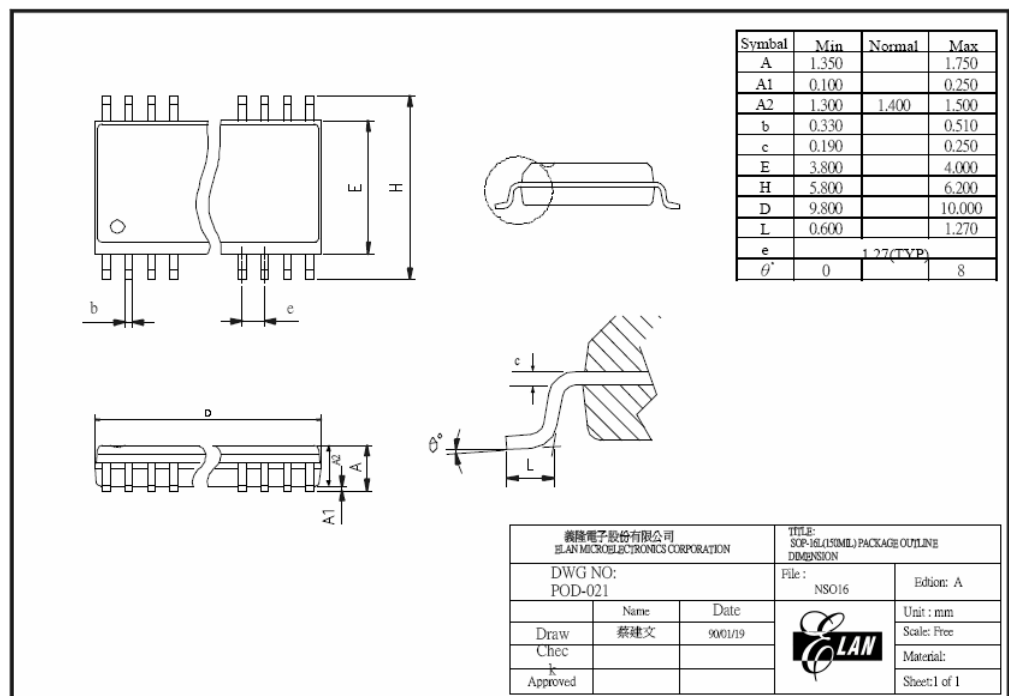
EM78M612ADP and EM78M612DDP



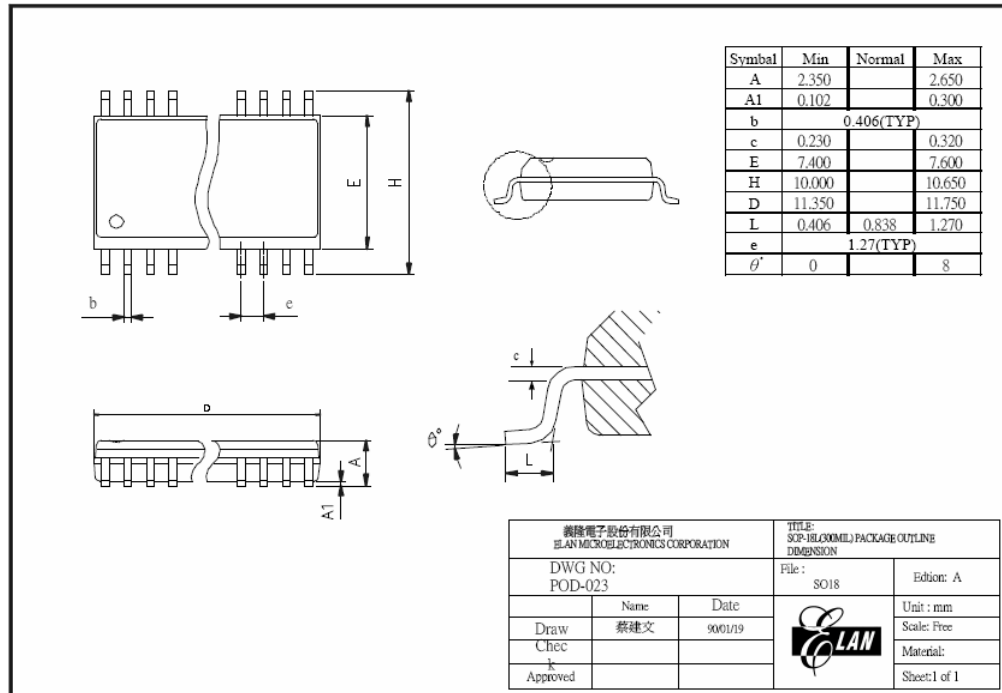
EM78M612ADK and EM78M612DDK



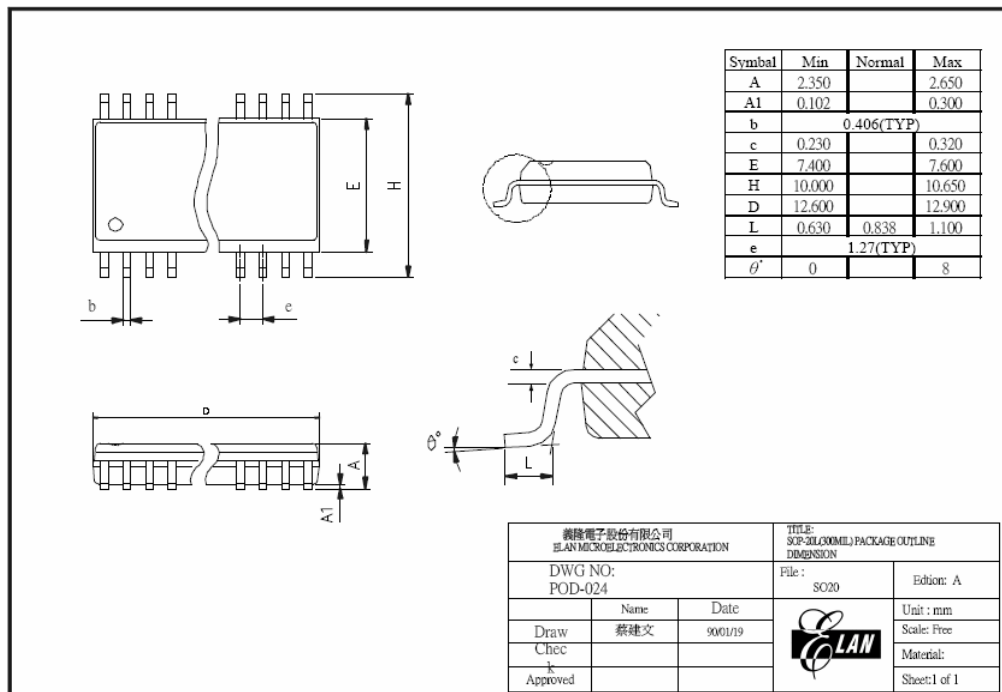
EM78M612AAM and EM78M612DAM



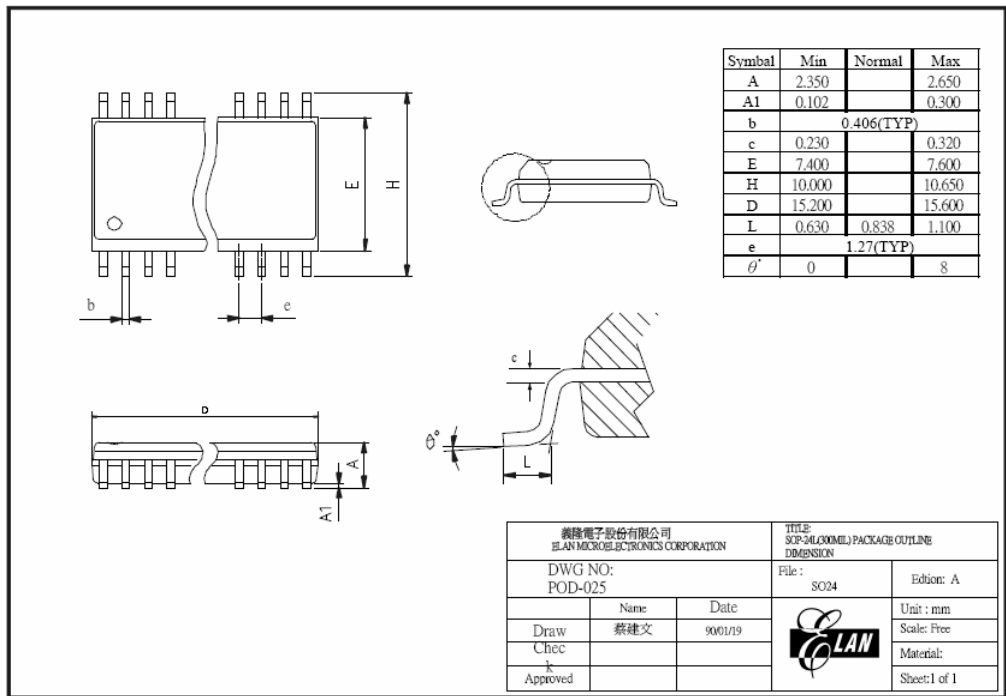
EM78M612ABM and EM78M612DBM



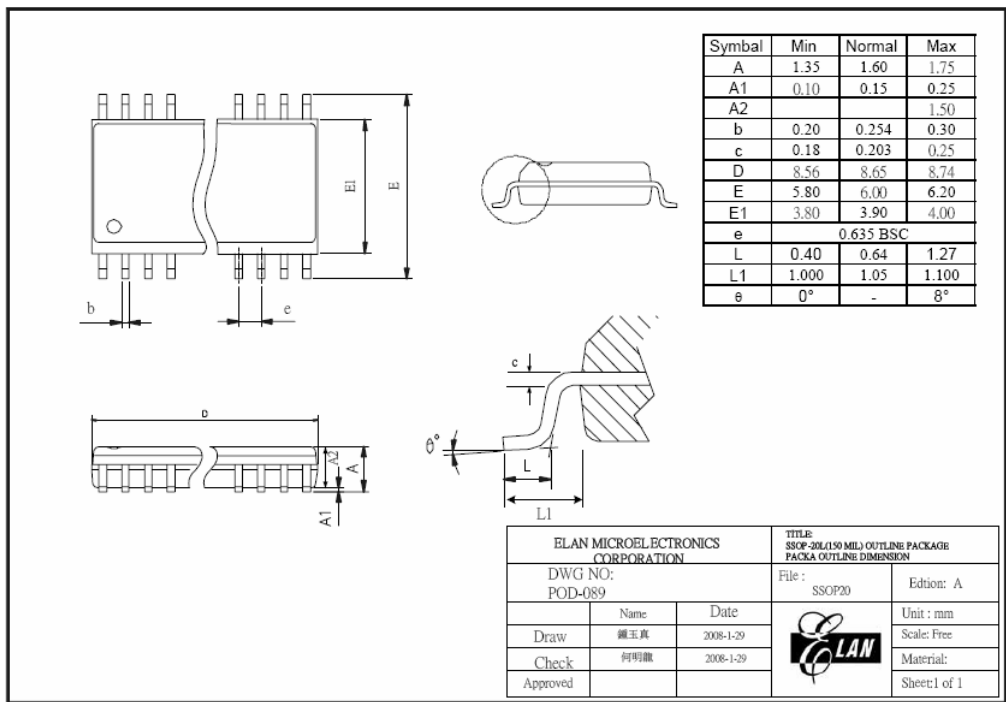
EM78M612ACM and EM78M612DCM



EM78M612ADM and EM78M612DDM

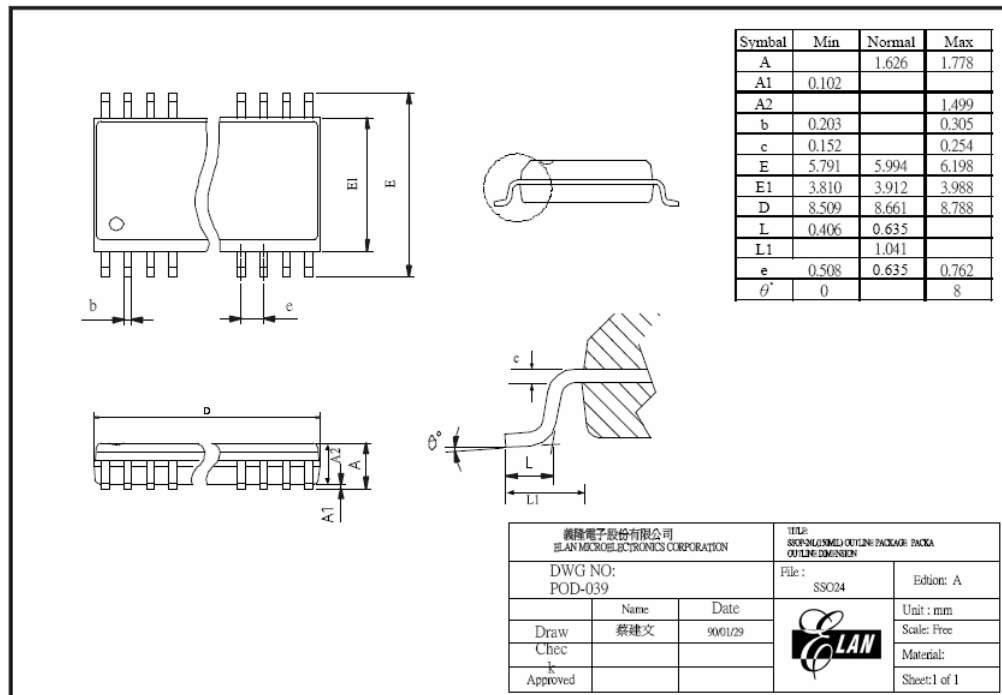


EM78M612AGM and EM78M612DGM

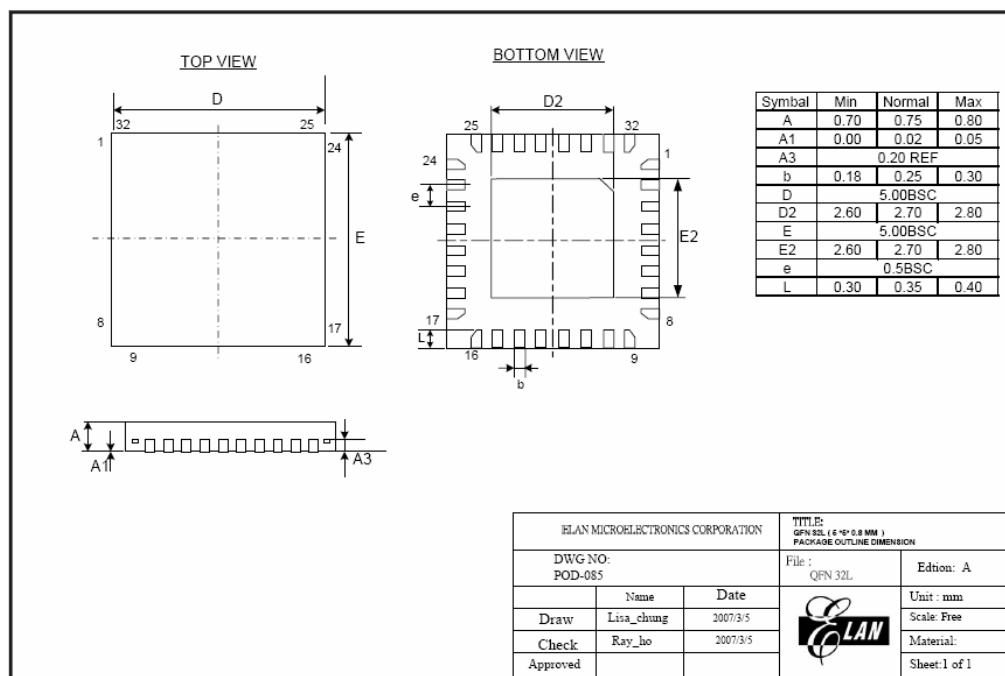




EM78M612AHM and EM78M612DHM



EM78M612AAW and EM78M612DAW



F MTP Program Pin

Use Elan's MTP (Multiple Time Programmable) writer to program the MTP IC. The following table lists the EM78M612 program pin in programming mode.

IC Pin Name	I/O	16-Pin Package	18-Pin Package	20-Pin Package	24-Pin Package	32-Pin Package
P60	P	16	1	1	1	5
P61	I	1	2	2	2	6
P62	I/O	2	3	3	3	7
P63	I	3	4	4	4	8
VSS	P	5	6	7	9	15, 24
VNN	P	6	7	8	10	17
OSCI	I	8	9	10	12	19
VDD	P	10	11	12	14	21
P64	I	15	18	20	24	4

